Southern Africa Large Telescope

Prime Focus Imaging Spectrograph

SAAO Detector Subsystem

Interface Control Document

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1 Scope

This document specifies the interfaces between the UW-Madison part of the Prime Focus Imaging Spectrograph (PFIS) and the SAAO-supplied Detector subsystem. The interfaces are optical, mechanical, electrical, cryogenic, software, and communications. There are no pneumatic interfaces between the Detector subsystem and PFIS. Figure 1 shows a block diagram with Figure 2 showing more detail in the SAAO detector subsystem.

Figure 1 shows the PFIS/SALT block diagram.
Figure 2 shows the SAAO part of Figure 1 in more detail.
Note that PFIS presents a single interface to the facility. Resources required by the PFIS subsystems (detector assembly and the etalons) are routed from the PFIS interface within the instrument. This is required for designing the PFIS wire harness.

2 Optical

The optical interface between PFIS and the Detector subsystem is defined to be the cryostat window. During assembly and thereafter, this will be the field lens, the final optical element, of the PFIS camera. However, for testing of the cryostat, the field lens will not be available in South Africa. In any case current test plans involve mounting the cryostat on the SAAO 1-m telescope. Thus, a separate, optically flat, cryostat window will be needed and is being procured from Mount Stromlo and Siding Spring Observatories.

3 Mechanical

This section specifies the mechanical interface between the PFIS and the Detector subsystem.

Figure 2 shows the mechanical design of the PFIS cryostat. UW are to provide SAAO with details of the interface to the PFIS camera structure.

3.1 Weight Budget

The Detector subsystem has a weight budget of TBD1 kg.

The array controller power supply (including 3m cable) has a weight budget of 6kg.

The array controller (populated with 4 pcb’s) has a weight budget of 6.5kg.

The detector housing (cryostat) has a weight budget of 9kg.

The ion pump controller has a weight budget of 1.8 kg.

The subsystems controller (including its power supply) has a weight budget of 4.0 kg.

Cabling has a weight budget of 1.0 kg.

3.2 Envelope

Figure 3 shows the mechanical envelope for the detector housing, measuring 185 x 205 x 215 mm. Allow an addition ~50 mm at ends carrying plugs.

Figure 4 shows the mechanical envelope for the array controller, measuring 360 x 175 x 140 mm. If the controller is to be fitted with a heat exchanger and insulated (see section 5), this envelope will have to be increased to 360 x 190 x 140 mm. An additional 20 mm on all three dimensions will be needed for the insulation.

Figure 5 shows the mechanical envelope for the power supply, measuring 250 x 200 x 110mm.
Figure 3 shows the current conceptual PFIS cryostat envelope and mounting point.
Figure 4 shows the SDSU II array controller envelope and mounting point.

Figure 5 shows the SDSU II power supply envelope and mounting point.
Figure 6 shows the Sub-systems Controller and Power Supply box envelope and mounting point.

Figure 7 shows the Varian MicroVac Ion Pump Controller envelope and mounting point.
Figure 6 shows the mechanical envelope of the subsystems controller, measuring 250 x 230 x 120 mm.

Figure 7 shows the mechanical envelope of the ion pump controller, measuring 107 x 130 x 164 mm.

3.3 Centre of Gravity
The CG of the array controller shall lie within a volume of 15 x 15 x 15 mm centred on the locations as depicted in Figure 8. This must be updated if the heat exchanger type of controller is used.

The CG of the power supply shall lie within a volume of 10 x 10 x 10 mm centred on the locations as depicted in Figure 9.

The CG of the detector housing shall lie within a volume of 10 x 10 x 10 mm, measured 50 ± 5 mm with respect to its mount point as depicted in Figure 10.

3.4 Mount Points
Figure 3 shows the detector housing mount plane being co-incidental with the optical focal plane as a 3-point kinematic system (ball-and-groove), centered on the optical axis, 35 mm behind the front surface of the cryostat window.

Figure 4 shows the array controller mount point consisting of eight holes, tapped M6. Two of the holes at the fans are unusable (see Figure 4). Note that the end connecting to the detector housing has a connector length limit of 2000 mm wire length.

Figure 5 shows the power supply mount point consisting of 4 x M6 clearance holes.

Figure 6 shows the subsystems controller mount point consisting of 4 x M5 clearance holes.

Figure 7 shows the ion pump controller mount point.

3.5 Handling Fixtures
The Detector Subsystem components shall accommodate cranes and hoists with suitably placed 1/2-13 threaded holes. Their location will depend on the detailed mechanical design, but should allow the components to be lifted in an attitude suitable for integration with the PFIS structure.

3.6 Shipping Container
The Detector Subsystem components shall be delivered to UW in a container suitable for reuse in shipping the components to South Africa. The shipping container(s) shall provide for the safe transport of the components, and any tools and fixtures required to assemble, install, remove, and disassemble the Detector subsystem; it will be suitable for any combination of road, rail, air, or sea transportation.
Figure 8 shows the centre of gravity of the SDSU II array controller. (Update if the heat exchanger version is to be used).

Figure 9 shows the centre of gravity of the SDSU II power supply.
Figure 10 shows the centre of gravity of the detector housing.

<table>
<thead>
<tr>
<th>SYSTEM</th>
<th>LOCATION</th>
<th>VOLTAGE</th>
<th>POWER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array controller Power Supply</td>
<td>Payload</td>
<td>*UPS 220v</td>
<td>0.15 kW</td>
</tr>
<tr>
<td>Ion Pump Controller</td>
<td>Payload</td>
<td>UPS 220v</td>
<td>0.04 kW</td>
</tr>
<tr>
<td>Sub-Systems Controller Power Supply</td>
<td>Payload</td>
<td>UPS 220v</td>
<td>0.1 kW TBC1</td>
</tr>
</tbody>
</table>

*UPS = “Detector” UPS power.

Table 1: Systems power requirements for SALTICAM
4 Electrical
This section specifies the electrical interface between the PFIS and the Detector subsystem.

4.1 Electrical Power
Electrical power is provided by the facility and is described in the PFIS-PFIP ICD. Power requirements are listed in Table 1.

The mains power to the array controller is to be “clean” UPS power while the Cryotiger compressor is to be supplied from “dirty” UPS power. The clean UPS mains power will be fed to the SDSU power supply which will in turn provide power to the array controller and detector. The SDSU/CCD system must NOT be remotely controllable in order to avoid inadvertent switching off. Manual switch on/off only.

4.2 Electrical Connectors
The Detector subsystem shall use the same style electrical connectors as PFIS. The type is IEC type.

4.3 Signal Connectors
The array controller is connected to its host computer via a dual optical fibre bundle (labeled Twin Fibre in Figure 1). This bundle shall be routed through the tracker wrap-up and will pass through the PFIS master interface panel without any interruption, i.e. the fibre optic is a point-to-point connection between the array controller on the one end and the host computer on the other end.

The fiber connector type is as supplied by ARC (Astronomical Research Cameras).

The array controller will also be connected to the detector cryostat by a cable no more than 2000 mm in length.

4.4 Shutter Control
The SDSU array controller uses one control signal for shutter open/close commands. A logic value of 0 will instruct the shutter to open, and a value of 1 to close.

Two TTL level shutter status signals will indicate that the shutter is in its fully open (logic 0) and fully closed position (logic 1).

The PFIS wire harness shall include wires for these signals. All electrical signals between the array controller and PFIS shall be optically isolated. The array controller connector type is TBD4.
5 Dry Air

In order to prevent the detector cryostat window from misting over, a dry air purge is applied. The dry instrument air, as supplied by the facility will be clean enough for this purpose. The optics purge overpressure exit may act as the window dry air purge.

6 Cryogenic and Refrigeration

The Detector subsystem requires both cryogenic cooling for the detector housing, and refrigeration for heat disposal from the power supply and array controller.

The cryotiger hose shall be routed from the Igloo, up through the tracker wrap-up (update with David Buckley’s comments at SALTICAM VI FDR), and then to the PFIS master interface panel. Note that although this hose is relatively flexible to bend, it does not allow any movement in twist. This hose shall be a combination of flexible stainless steel hose (as supplied by the cryotiger manufacturer) and solid copper tubing to enable disconnection for maintenance purposes. The panel connector type is TBD5. The cryocoolant will be routed through the PFIS to the detector housing. The detector housing connector type is TBD6.

The facility shall deliver glycol coolant to the PFIS master interface panel. The connector is specified in the PFIS/SALT ICD.

The glycol shall be routed within the PFIS to the locations of the power supply, the array controller, the ion pump controller and the subsystems controller. The cooled components shall use the same type of connector. The type of connector is TBD7.

In addition to the array controller, the ion pump controller and subsystems controller and the SDSU power supply will need cooling.

There are two possibilities of implementing the cooling of power supplies and controller units (TBD8) – either using a standard “SALT cooler box” (probably the best option for everything but the array controller. This solution is depicted in Fig. 2) or modify one or more external surface(s) to be a glycol heat exchanger and insulate the complete component (probably the best option for the array controller – most probably the side marked “HOT SIDE” in Figure 4). Although the array controller is shown in Fig. 2 as in the cooler box, if the heat exchanger option is used it will not be in the cooler box.

We must define who is responsible for the cooler box – are these items going in a common box with PFIS stuff? Are they going in a separate box? Also someone has to design & have built a cooler box for the SDSU controller. The details of this enclosure must go in the ICD.

7 Computers and Communications (TBD14)

This section specifies the computer and communications interface between the PFIS and the Detector subsystem.

The array controller will be controlled with LabView on a Linux or “Real Time” (RT) Linux PC with a PCI backplane (labelled SAAO PC in Figure 1). The LabView front end will communicate with a RT Linux Module which will control the array controller.
Communications between the PFIS and/or its control PC and the Detector Subsystem will be on Ethernet, under the control of LabView's network communications protocol. The Detector Subsystem will provide (via standard LabView protocols) all relevant information about itself. The details are TBD9.

8 Software (TBD14)

This section specifies the software interface between the PFIS and the Detector Subsystem.

Both the PFIS and the Detector Subsystem will be controlled by LabView running under Linux.

PFIS requires certain image readout and processing functions in order to perform real-time operations such as telescope pointing and peakup, detector calibrations, and image quality assessment.

8.1 Subarrays

TO BE DISCUSSED, TAKING CONTROLLER HARDWARE IMPLICATIONS INTO ACCOUNT.

The Detector Subsystem will support rapid readout and processing of 20 PFIS-selectable subarrays on the CCD. The subarrays can be of any size, but may not be overlapping. (DEFINITION OF OVERLAPPING WINDOWS TO BE REPHRASED). They will be specified on the fly, and may be changed at any time between readouts.

Subarray processing includes determining the background, summing the counts above the background, and prebinning in either dimension. The total counts and count rate in the subarrays will be sent to the PFIS within 1 second of the readout request.

8.2 Readout Modes

The Detector Subsystem will provide readout modes compatible with the OCDD. Details will be in the software documents. All readouts will be time-tagged to an accuracy of one millisecond (TBD10). In all cases, the Detector Subsystem will send a readout complete message to PFIS, which may choose to block during an integration and unblock upon completion.

- Asynchronous (Upon request). In this mode, PFIS will issue a command to do an exposure sequence of a defined integration time and some time later will request the image data via LabView's network communications protocol. Integration will begin within TBD11 milliseconds of receiving the request.
- Synchronous (Rapid, periodic). In this mode, the PFIS will set an integration time and a frame count, and when told to begin, the Detector Subsystem will commence readouts at the programmed rate. The interframe timing jitter will be less than TBD12 milliseconds. The PFIS may stop the readout sequence before the frame count has been reached. If halted during a readout, the Detector Subsystem will finish the
current frame and not begin another. This allows PFIS to end a time-resolved imaging sequence without having to know the details of where the Detector Subsystem is in its operation. The frame count may be 1, and the integration time may vary from the fastest possible readout time to the longest possible time on target (hours).

Details of this are still to be confirmed/finalized between UW and SAAO.

8.3 Commands
The Detector subsystem will execute high level commands such as:

- Do a “prepare readout” (i.e. clear out the CCDs).
- Do a $n$ seconds exposure.
- Do a $n$ seconds dark exposure (i.e. without opening the shutter).
- Change pre-bin mode to $m \times n$ for subsequent frames, where $1 \leq m \leq 9$ and $1 \leq n \leq 9$.
- Subarray (window) multiple up to TBD13 (WE WOULD LIKE TO PROPOSE A MAXIMUM OF 10 WINDOWS. IS THIS OK?).
- Status/telemetry request.

Details of this are still to be confirmed/finalized between UW and SAAO.

8.4 Telemetry
The Detector LabView VI shall provide, via standard LabView methods, the following information.

- Array controller mode (e.g. Standby, Ready, Busy, Error, etc).
- CCD temperature.
- Cryotiger (cold plate) temperature.
- Internal temperature of array controller.
- Ion pump pressure reading.
- CCD temperature-servo-heater power dissipation (indirect check on vacuum quality).
- Shutter closed/open status.
- Frame mode (e.g. Full frame, Frame transfer, “Masked” frame, etc).
- Pre-binning mode.
- Integration time left.

Details of this are still to be confirmed/finalized between UW and SAAO.
## 9 List of TBD And TBCs

<table>
<thead>
<tr>
<th>TBD</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TBD1</td>
<td>Weight budget for Detector subsystem</td>
</tr>
<tr>
<td>TBD2</td>
<td></td>
</tr>
<tr>
<td>TBD3</td>
<td></td>
</tr>
<tr>
<td>TBD4</td>
<td>Array controller connector type</td>
</tr>
<tr>
<td>TBD5</td>
<td>PFIS Master Interface Panel connector type</td>
</tr>
<tr>
<td>TBD6</td>
<td>Detector housing connector type</td>
</tr>
<tr>
<td>TBD7</td>
<td>Cooled unit connector type</td>
</tr>
<tr>
<td>TBD8</td>
<td>Alternative cooling schemes for array controller and its power supply</td>
</tr>
<tr>
<td>TBD9</td>
<td>Detector subsystem status information packet</td>
</tr>
<tr>
<td>TBD10</td>
<td>Accuracy of time-tagging of readouts</td>
</tr>
<tr>
<td>TBD11</td>
<td>Time lag between receiving request for asynchronous exposure and start of exposure</td>
</tr>
<tr>
<td>TBD12</td>
<td>Interframe timing jitter</td>
</tr>
<tr>
<td>TBD13</td>
<td>Subarray multiple</td>
</tr>
<tr>
<td>TBD14</td>
<td>All aspects of communications of commands, status and data between the Detector Subsystem PC and the PFIS PC or PFIS block in Figure 1</td>
</tr>
<tr>
<td>TBC1</td>
<td>Subsystem controller power requirement.</td>
</tr>
</tbody>
</table>