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FTP Site: ftp.natinst.com
Web Address: www.natinst.com

Bulletin Board Support
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BBS United Kingdom: 01635 551422
BBS France: 01 48 65 15 59

Fax-on-Demand Support
512 418 1111

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Tel: 512 795 8248
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Canada (Ontario) 905 785 0085, Canada (Québec) 514 694 8521, Denmark 45 76 26 00, Finland 09 725 725 11,
France 01 48 14 24 24, Germany 089 741 31 30, Hong Kong 2645 3186, Israel 03 6120092, Italy 02 413091,
Japan 03 5472 2970, Korea 02 596 7456, Mexico 5 520 2635, Netherlands 0348 433466, Norway 32 84 84 00,
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About This Manual

This manual describes the electrical and mechanical aspects of each board in the PXI E Series product line and contains information concerning their operation and programming. Unless otherwise noted, text applies to all boards in the PXI E Series.

The PXI E Series includes the following boards:
• PXI-6030E
• PXI-6031E
• PXI-6040E
• PXI-6070E
• PXI-6071E

The PXI E Series boards are high-performance multifunction analog, digital, and timing I/O boards for PXI bus computers. Supported functions include analog input, analog output, digital I/O, and timing I/O.

Organization of This Manual

The PXI E Series User Manual is organized as follows:
• Chapter 1, Introduction, describes the PXI E Series boards, lists what you need to get started, describes the optional software and optional equipment, and explains how to unpack your PXI E Series board.
• Chapter 2, Installation and Configuration, explains how to install and configure your PXI E Series board.
• Chapter 3, Hardware Overview, presents an overview of the hardware functions on your PXI E Series board.
• Chapter 4, Signal Connections, describes how to make input and output signal connections to your PXI E Series board via the board I/O connector.
• Chapter 5, Calibration, discusses the calibration procedures for your PXI E Series board.
• Appendix A, Specifications, lists the specifications of each PXI E Series board.
• Appendix B, Optional Cable Connector Descriptions, describes the connectors on the optional cables for the PXI E Series boards.
About This Manual

- Appendix C, *Common Questions*, contains a list of commonly asked questions and their answers relating to usage and special features of your PXI E Series board.
- Appendix D, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, and symbols.
- The *Index* contains an alphabetical list of key terms and topics in this manual, including the page where you can find each one.

Conventions Used in This Manual

The following conventions are used in this manual.

<>
Angle brackets enclose the name of a key on the keyboard—for example, <shift>. Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DBIO<3..0>.

,unsigned
The ♦ symbol indicates that the text following it applies only to specific PXI E Series boards.

This icon to the left of bold italicized text denotes a note, which alerts you to important information.

This icon to the left of bold italicized text denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.

Bold text denotes parameters.

**bold italic**
Bold italic text denotes a note, caution, or warning.

CompactPCI
Refers to the core specification defined by the PCI Industrial Computer Manufacturer’s Group (PICMG)

*italic*
Italic text denotes emphasis on a specific board in the PXI E Series or on other important information, a cross reference, or an introduction to a key concept.

**monospace**
Text in this font denotes text or characters that you should literally enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths,
directories, programs, subprograms, subroutines, device names, functions, variables, file names, and extensions, and for statements and comments taken from program code.

NI-DAQ

NI-DAQ refers to the NI-DAQ driver software for Macintosh or PC compatible computers unless otherwise noted.

PC

Refers to all PC AT series computers with PXI bus unless otherwise noted.

PXI

Stands for PCI eXtensions for Instrumentation. PXI is an open specification that builds off the CompactPCI specification by adding instrumentation-specific features.

SCXI

SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ boards.

National Instruments Documentation

The *PXI E Series User Manual* is one piece of the documentation set for your DAQ system. You could have any of several types of manuals depending on the hardware and software in your system. Use the manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.

- Your SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.

- Your DAQ hardware documentation—This documentation has detailed information about the DAQ hardware that plugs into or is connected to your computer. Use this documentation for hardware installation and configuration instructions, specification information about your DAQ hardware, and application hints.

- Software documentation—You may have both application software and NI-DAQ software documentation. National Instruments application software includes ComponentWorks, LabVIEW, LabWindows/CVI, Measure, and VirtualBench. After you set up your hardware system, use either your application software documentation or the NI-DAQ documentation to help you write your application. If
you have a large, complicated system, it is worthwhile to look through the software documentation before you configure your hardware.

- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.

- *SCXI Chassis Manual*—If you are using SCXI, read this manual for maintenance information on the chassis and installation instructions.

**Related Documentation**

The following documents contain information you may find helpful:

- *DAQ-STC Technical Reference Manual*
- National Instruments Application Note 025, *Field Wiring and Noise Considerations for Analog Signals*
- *PCI Local Bus Specification Revision 2.1*
- *PICMG CompactPCI 2.0 R2.1*
- *PXI Specification Revision 1.0*

**Customer Communication**

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix D, *Customer Communication*, at the end of this manual.
Introduction

This chapter describes the PXI E Series boards, lists what you need to get started, describes the optional software and optional equipment, and explains how to unpack your PXI E Series board.

About the PXI E Series

Thank you for buying a National Instruments PXI E Series board. The PXI E Series boards are completely Plug and Play, multifunction analog, digital, and timing I/O boards for PXI. This family of boards features 12-bit and 16-bit ADCs with 16 analog inputs, 12-bit and 16-bit DACs with voltage outputs, eight lines of TTL-compatible digital I/O, and two 24-bit counter/timers for timing I/O. Because the PXI E Series boards have no DIP switches, jumpers, or potentiometers, they are easily software-configured and calibrated.

The PXI E Series boards are completely switchless and jumperless data acquisition (DAQ) boards. This feature is made possible by the National Instruments MITE bus interface chip that connects the board to the PXI bus. The MITE implements the PCI Local Bus Specification so that the interrupts and base memory addresses are all software configured.

The PXI E Series boards use the National Instruments DAQ-STC system timing controller for time-related functions. The DAQ-STC consists of three timing groups that control analog input, analog output, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns. The DAQ-STC makes possible such applications as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate.

Often with DAQ boards, you cannot easily synchronize several measurement functions to a common trigger or timing event. The PXI-MIO E Series boards have the Real-Time System Integration (RTSI) bus to solve this problem. The RTSI bus consists of our RTSI bus interface and the PXI Trigger signals on the PXI backplane to route timing and trigger signals between several functions on as many as seven DAQ boards in your system.
The PXI E Series boards can interface to an SCXI system so that you can acquire over 3,000 analog signals from thermocouples, RTDs, strain gauges, voltage sources, and current sources. You can also acquire or generate digital signals for communication and control. SCXI is the instrumentation front end for plug-in DAQ boards.

Detailed specifications of the PXI E Series boards are in Appendix A, Specifications.

Using PXI with CompactPCI

Using PXI compatible products with standard CompactPCI products is an important feature provided by PXI Specification Revision 1.0. If you use a PXI compatible plug-in card in a standard CompactPCI chassis, you will be unable to use PXI-specific functions, but you can still use the basic plug-in card functions. For example, the RTSI bus on your PXI E Series board is available in a PXI chassis, but not in a CompactPCI chassis.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI boards with different sub-buses nor between CompactPCI boards with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. Your PXI E Series board will work in any standard CompactPCI chassis adhering to PICMG CompactPCI 2.0 R2.1.

PXI specific features are implemented on the J2 connector of the CompactPCI bus. Table 1-1 lists the J2 pins used by your PXI E Series board. Your PXI board is compatible with any Compact PCI chassis with a sub-bus that does not drive these lines. Even if the sub-bus is capable of driving these lines, the PXI board is still compatible as long as those pins on the sub-bus are disabled by default and not ever enabled. Damage may result if these lines are driven by the sub-bus.

<table>
<thead>
<tr>
<th>PXI E Series Signal</th>
<th>PXI Pin Name</th>
<th>PXI J2 Pin Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTSI&lt;0..5&gt;</td>
<td>PXI Trigger&lt;0..5&gt;</td>
<td>B16, A16, A17, A18, B18, C18</td>
</tr>
<tr>
<td>RTSI 6</td>
<td>PXI Star</td>
<td>D17</td>
</tr>
<tr>
<td>RTSI Clock</td>
<td>PXI Trigger 7</td>
<td>E16</td>
</tr>
</tbody>
</table>
To set up and use your PXI E Series board, you will need the following:

- One of the following boards:
  - PXI-6030E
  - PXI-6031E
  - PXI-6040E
  - PXI-6070E
  - PXI-6071E

- PXI E Series User Manual

- One of the following software packages and documentation:
  - ComponentWorks
  - LabVIEW for Windows
  - LabWindows/CVI for Windows
  - Measure
  - NI-DAQ for PC Compatibles
  - VirtualBench

- Your PXI or CompactPCI chassis and controller (hereafter referred to as your computer)

Software Programming Choices

You have several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use National Instruments application software, NI-DAQ, or register-level programming.
National Instruments Application Software

ComponentWorks contains tools for data acquisition and instrument control built on NI-DAQ driver software. ComponentWorks provides a higher-level programming interface for building virtual instruments through standard OLE controls and DLLs. With ComponentWorks, you can use all of the configuration tools, resource management utilities, and interactive control utilities included with NI-DAQ.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to NI-DAQ software.

LabWindows/CVI features interactive graphics, state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition Library is functionally equivalent to the NI-DAQ software.

VirtualBench features virtual instruments that combine DAQ products, software, and your computer to create a stand-alone instrument with the added benefit of the processing, display, and storage capabilities of your computer. VirtualBench instruments load and save waveform data to disk in the same forms that can be used in popular spreadsheet programs and word processors.

Using ComponentWorks, LabVIEW, LabWindows/CVI, or VirtualBench software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with SCXI or accessory products, except for the SCXI-1200. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation (timed D/A conversion), digital I/O, counter/timer operations, SCXI, RTSI, self-calibration, messaging, and acquiring data to extended memory.
NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you are using conventional programming languages or National Instruments application software, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

![Diagram](image)

**Figure 1-1.** The Relationship between the Programming Environment, NI-DAQ, and Your Hardware
Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient, and is not recommended for most users.

Even if you are an experienced register-level programmer, using NI-DAQ or application software to program your National Instruments DAQ hardware is easier than, and as flexible as, register-level programming, and can save weeks of development time.

Optional Equipment

National Instruments offers a variety of products to use with your PXI E Series board, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded 50-, 68-, and 100-pin screw terminals
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3,072 channels.
- Low channel count signal conditioning modules, boards, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays

For more specific information about these products, refer to your National Instruments catalogue or call the office nearest you.

Custom Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change board interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

- For the analog input signals, shielded twisted-pair wires for each analog input pair yield the best results, assuming that you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
• You should route the analog lines separately from the digital lines.
• When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

The following list gives recommended part numbers for connectors that mate to the I/O connector on your PXI E Series board.

♦ PXI-6030E, PXI-6040E, PXI-6070E
  • Honda 68-position, solder cup, female connector (part number PCS-E68FS)
  • Honda backshell (part number PCS-E68LKPA)

For more information on mating connectors and a backshell kit for making custom 68-pin cables, see the National Instruments Catalogue.

♦ PXI-6031E and PXI-6071E
  • AMP 100-position IDC male connector (part number 1-750913-9)
  • AMP backshell, 0.50 max O.D. cable (part number 749081-1)
  • AMP backshell, 0.55 max O.D. cable, (part number 749854-1)

Unpacking

Your PXI E Series board is shipped in an antistatic package to prevent electrostatic damage to the board. Electrostatic discharge can damage several components on the board. To avoid such damage in handling the board, take the following precautions:

• Ground yourself via a grounding strap or by holding a grounded object.
• Touch the antistatic package to a metal part of your computer chassis before removing the board from the package.
• Remove the board from the package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. Do not install a damaged board into your computer.
• Never touch the exposed pins of connectors.
Installation and Configuration

This chapter explains how to install and configure your PXI E Series board.

Software Installation

Install your software before you install your PXI E Series board. Refer to the appropriate release notes indicated below for specific instructions on the software installation sequence.

If you are using NI-DAQ, refer to your NI-DAQ release notes. Find the installation section for your operating system and follow the instructions given there.

If you are using LabVIEW, LabWindows/CVI, or other National Instruments application software packages, refer to the appropriate release notes. After you have installed your application software, refer to your NI-DAQ release notes and follow the instructions given there for your operating system and application software package.

Hardware Installation

You can install a PXI E Series board in any available expansion slot in your computer. However, to achieve best noise performance, leave as much room as possible between the PXI E Series board and other boards and hardware. The following are general installation instructions, but consult your computer user manual or technical reference manual for specific instructions and warnings.

1. Write down the PXI E Series board serial number in the PXI E Series Hardware and Software Configuration Form in Appendix D, Customer Communication, of this manual.

2. Turn off and unplug your computer.

3. Choose an unused PXI slot in your system. For maximum performance, the PXI E Series board has an onboard DMA controller that can only be used if the board is installed in a slot that supports bus arbitration, or bus master cards. National Instruments recommends installing the PXI E Series board in such a slot. The PXI specification
requires all slots to support bus master cards, but the CompactPCI specification does not. If you install in a CompactPCI non-master slot, you must disable the PXI E Series board onboard DMA controller using software.

4. Remove the filler panel for the slot you have chosen.

5. Insert the PXI E Series board into a 5 V PXI slot. Use the injector/ejector handle to fully insert the board into the chassis.

6. Screw the front panel of the PXI E Series board to the front panel mounting rail of the system.

7. Plug in and turn on your computer.

The PXI E Series board is installed. You are now ready to configure your software. Refer to your software documentation for configuration instructions.

**Board Configuration**

Due to the National Instruments standard architecture for data acquisition and the PXI bus specification, the PXI E Series boards are completely software configurable. You must perform two types of configuration on the PXI E Series boards—bus-related and data acquisition-related configuration.

The PXI E Series boards are fully compatible with the *PXI Specification Revision 1.0*. This allows the PXI system to automatically perform all bus-related configurations and requires no user interaction. Bus-related configuration includes setting the board base memory address and interrupt channel.

Data-acquisition-related configuration includes such settings as analog input polarity and range, analog input mode, and others. You can modify these settings through application level software, such as NI-DAQ, ComponentWorks, LabVIEW, LabWindows/CVI, and VirtualBench.
This chapter presents an overview of the hardware functions on your PXI E Series board.

Figure 3-1 shows a block diagram for the PXI-6040E, PXI-6070E, and PXI-6071E.

Figure 3-1. PXI-6040E, PXI-6070E, and PXI-6071E Block Diagram
Figure 3-2 shows a block diagram for the PXI-6030E and PXI-6031E.

![Figure 3-2. PXI-6030E and PXI-6031E Block Diagram](image)

**Analog Input**

The analog input section of each PXI E Series board is software configurable. You can select different analog input configurations through application software designed to control the PXI E Series boards. The following sections describe in detail each of the analog input categories.

**Input Mode**

The PXI E Series boards have three different input modes—nonreferenced single-ended (NRSE) input, referenced single-ended (RSE) input, and differential (DIFF) input. The single-ended input configurations provide up to 16 channels (64 channels on the PXI-6031E and PXI-6071E). The DIFF input configuration provides up to eight channels (32 channels on the PXI-6031E and PXI-6071E). Input modes are programmed on a per channel basis for multimode scanning. For example, you can configure the
circuitry to scan 12 channels—four differentially-configured channels and eight single-ended channels. Table 3-1 describes the three input configurations.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIFF</td>
<td>A channel configured in DIFF mode uses two analog channel input lines. One line connects to the positive input of the board programmable gain instrumentation amplifier (PGIA), and the other connects to the negative input of the PGIA.</td>
</tr>
<tr>
<td>RSE</td>
<td>A channel configured in RSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA is internally tied to analog input ground (AIGND).</td>
</tr>
<tr>
<td>NRSE</td>
<td>A channel configured in NRSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA connects to the analog input sense (AISENSE) input.</td>
</tr>
</tbody>
</table>

For more information about the three types of input configuration, refer to the Analog Input Signal Connections section in Chapter 4, Signal Connections, which contains diagrams showing the signal paths for the three configurations.

### Input Polarity and Input Range

- PXI-6040E, PXI-6070E, and PXI-6071E

These boards have two input polarities—unipolar and bipolar. Unipolar input means that the input voltage range is between 0 and $V_{\text{ref}}$, where $V_{\text{ref}}$ is a positive reference voltage. Bipolar input means that the input voltage range is between $-V_{\text{ref}}/2$ and $+V_{\text{ref}}/2$. These boards have a unipolar input range of 10 V (0 to 10 V) and a bipolar input range of 10 V ($\pm 5$ V).

You can program polarity and range settings on a per channel basis so that you can configure each input channel uniquely.

The software-programmable gain on these boards increases their overall flexibility by matching the input signal ranges to those that the ADC can accommodate. These boards have gains of 0.5, 1, 2, 5, 10, 20, 50, and 100.
and are suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-2 shows the overall input range and precision according to the input range configuration and gain used.

Table 3-2. Actual Range and Measurement Precision, PXI-6040E, PXI-6070E, and PXI-6071E

<table>
<thead>
<tr>
<th>Range Configuration</th>
<th>Gain</th>
<th>Actual Input Range</th>
<th>Precision 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to +10 V</td>
<td>1.0</td>
<td>0 to +10 V</td>
<td>2.44 mV</td>
</tr>
<tr>
<td></td>
<td>2.0</td>
<td>0 to +5 V</td>
<td>1.22 mV</td>
</tr>
<tr>
<td></td>
<td>5.0</td>
<td>0 to +2 V</td>
<td>488.28 µV</td>
</tr>
<tr>
<td></td>
<td>10.0</td>
<td>0 to +1 V</td>
<td>244.14 µV</td>
</tr>
<tr>
<td></td>
<td>20.0</td>
<td>0 to +500 mV</td>
<td>122.07 µV</td>
</tr>
<tr>
<td></td>
<td>50.0</td>
<td>0 to +200 mV</td>
<td>48.83 µV</td>
</tr>
<tr>
<td></td>
<td>100.0</td>
<td>0 to +100 mV</td>
<td>24.41 µV</td>
</tr>
<tr>
<td>–5 to +5 V</td>
<td>0.5</td>
<td>–10 to +10 V</td>
<td>4.88 mV</td>
</tr>
<tr>
<td></td>
<td>1.0</td>
<td>–5 to +5 V</td>
<td>2.44 mV</td>
</tr>
<tr>
<td></td>
<td>2.0</td>
<td>–2.5 to +2.5 V</td>
<td>1.22 mV</td>
</tr>
<tr>
<td></td>
<td>5.0</td>
<td>–1 to +1 V</td>
<td>488.28 µV</td>
</tr>
<tr>
<td></td>
<td>10.0</td>
<td>–500 to +500 mV</td>
<td>244.14 µV</td>
</tr>
<tr>
<td></td>
<td>20.0</td>
<td>–250 to +250 mV</td>
<td>122.07 µV</td>
</tr>
<tr>
<td></td>
<td>50.0</td>
<td>–100 to +100 mV</td>
<td>48.83 µV</td>
</tr>
<tr>
<td></td>
<td>100.0</td>
<td>–50 to +50 mV</td>
<td>24.41 µV</td>
</tr>
</tbody>
</table>

1 The value of 1 LSB of the 12-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 12-bit count.

Note: See Appendix A, Specifications, for absolute maximum ratings.

♦ PXI-6030E and PXI-6031E

These boards have two input polarities—unipolar and bipolar. Unipolar input means that the input voltage range is between 0 and $V_{ref}$, where $V_{ref}$ is a positive reference voltage. Bipolar input means that the input voltage range is between $-V_{ref}$ and $+V_{ref}$. So, these boards have a unipolar input range of 10 V (0 to 10 V) and a bipolar input range of 20 V ($\pm$10 V). You can program polarity and range settings on a per channel basis so that you can configure each input channel uniquely.
You can calibrate your PXI-6030E and PXI-6031E analog input circuitry for either a unipolar or bipolar polarity. If you mix unipolar and bipolar channels in your scan list and you are using NI-DAQ, then NI-DAQ will load the calibration constants appropriate to the polarity for which analog input channel 0 is configured.

The software-programmable gain on these boards increases their overall flexibility by matching the input signal ranges to those that the ADC can accommodate. These boards have gains of 1, 2, 5, 10, 20, 50, and 100. These gains are suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal.

Table 3-3 shows the overall input range and precision according to the input range configuration and gain used.

<table>
<thead>
<tr>
<th>Range Configuration</th>
<th>Gain</th>
<th>Actual Input Range</th>
<th>Precision $^1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to +10 V</td>
<td>1.0</td>
<td>0 to +10 V</td>
<td>152.59 µV</td>
</tr>
<tr>
<td></td>
<td>2.0</td>
<td>0 to +5 V</td>
<td>76.29 µV</td>
</tr>
<tr>
<td></td>
<td>5.0</td>
<td>0 to +2 V</td>
<td>30.52 µV</td>
</tr>
<tr>
<td></td>
<td>10.0</td>
<td>0 to +1 V</td>
<td>15.26 µV</td>
</tr>
<tr>
<td></td>
<td>20.0</td>
<td>0 to +500 mV</td>
<td>7.63 µV</td>
</tr>
<tr>
<td></td>
<td>50.0</td>
<td>0 to +200 mV</td>
<td>3.05 µV</td>
</tr>
<tr>
<td></td>
<td>100.0</td>
<td>0 to 100 mV</td>
<td>1.53 µV</td>
</tr>
<tr>
<td>−10 to +10 V</td>
<td>1.0</td>
<td>−10 to +10 V</td>
<td>305.18 µV</td>
</tr>
<tr>
<td></td>
<td>2.0</td>
<td>−5 to +5 V</td>
<td>152.59 µV</td>
</tr>
<tr>
<td></td>
<td>5.0</td>
<td>−2 to +2 V</td>
<td>61.04 µV</td>
</tr>
<tr>
<td></td>
<td>10.0</td>
<td>−1 to +1 V</td>
<td>30.52 µV</td>
</tr>
<tr>
<td></td>
<td>20.0</td>
<td>−500 to +500 mV</td>
<td>15.26 µV</td>
</tr>
<tr>
<td></td>
<td>50.0</td>
<td>−200 to +200 mV</td>
<td>6.10 µV</td>
</tr>
<tr>
<td></td>
<td>100.0</td>
<td>−100 to +100 mV</td>
<td>3.05 µV</td>
</tr>
</tbody>
</table>

$^1$The value of 1 LSB of the 16-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 16-bit count.

Note: See Appendix A, Specifications, for absolute maximum ratings.
Considerations for Selecting Input Ranges

Which input polarity and range you select depends on the expected range of the incoming signal. A large input range can accommodate a large signal variation but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution but may result in the input signal going out of range. For best results, match the input range as closely as possible to the expected range of the input signal. For example, if you are certain the input signal will not be negative (below 0 V), unipolar input polarity is best. However, if the signal is negative or equal to zero, you will get inaccurate readings if you use unipolar input polarity.

Dither

When you enable dither, you add approximately 0.5 LSB\text{rms} of white Gaussian noise to the signal to be converted by the ADC. This addition is useful for applications involving averaging to increase the resolution of your PXI E Series board, as in calibration or spectral analysis. In such applications, noise modulation is decreased and differential linearity is improved by the addition of the dither. When taking DC measurements, such as when checking the board calibration, you should enable dither and average about 1,000 points to take a single reading. This process removes the effects of quantization and reduces measurement noise, resulting in improved resolution. For high-speed applications not involving averaging or spectral analysis, you may want to disable the dither to reduce noise. Your software enables and disables the dither circuitry.

Figure 3-3 illustrates the effect of dither on signal acquisition. Figure 3-3a shows a small (±4 LSB) sine wave acquired with dither off. The ADC quantization is clearly visible. Figure 3-3b shows what happens when 50 such acquisitions are averaged together; quantization is still plainly visible. In Figure 3-3c, the sine wave is acquired with dither on. There is a considerable amount of visible noise. But averaging about 50 such acquisitions, as shown in Figure 3-3d, eliminates both the added noise and the effects of quantization. Dither has the effect of forcing quantization noise to become a zero-mean random variable rather than a deterministic function of the input signal.
You cannot disable dither on the PXI-6030E or PXI-6031E. This is because the ADC resolution is so fine that the ADC and the PGIA inherently produce almost 0.5 LSB_{rms} of noise. This is equivalent to having a dither circuit that is always enabled.

**Multichannel Scanning Considerations**

Most of the PXI E Series boards can scan multichannels at the same maximum rate as their single-channel rate; however, pay careful attention to the settling times for each of the boards. The settling time for most of the PXI E Series boards is independent of the selected gain, even at the maximum sampling rate. The settling time for the very high-speed boards is gain dependent, which can affect the useful sampling rate for a given gain. No extra settling time is necessary between channels as long as the gain is constant and source impedances are low. Refer to Appendix A, *Specifications*, for a complete listing of settling times for each of the PXI E Series boards.
When scanning among channels at various gains, the settling times may increase. When the PGIA switches to a higher gain, the signal on the previous channel may be well outside the new, smaller range. For instance, suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1, and suppose the PGIA is programmed to apply a gain of one to channel 0 and a gain of 100 to channel 1. When the multiplexer switches to channel 1 and the PGIA switches to a gain of 100, the new full-scale range is 100 mV (if the ADC is in unipolar mode).

The approximately 4 V step from 4 V to 1 mV is 4,000% of the new full-scale range. For a 16-bit board to settle within 0.0015% (15 ppm or 1 LSB) of the 100 mV full-scale range on channel 1, the input circuitry has to settle within 0.00004% (0.4 ppm or 1/400 LSB) of the 4 V step. It may take as long as 200 µs for the circuitry to settle this much. In general, this extra settling time is not needed when the PGIA is switching to a lower gain.

Settling times can also increase when scanning high-impedance signals due to a phenomenon called charge injection, where the analog input multiplexer injects a small amount of charge into each signal source when that source is selected. If the impedance of the source is not low enough, the effect of the charge—a voltage error—will not have decayed by the time the ADC samples the signal. For this reason, keep source impedances under 1 kΩ to perform high-speed scanning.

Due to the previously described limitations of settling times resulting from these conditions, multichannel scanning is not recommended unless sampling rates are low enough or it is necessary to sample several signals as nearly simultaneously as possible. The data is much more accurate and channel-to-channel independent if you acquire data from each channel independently (for example, 100 points from channel 0, then 100 points from channel 1, then 100 points from channel 2, and so on).

**Analog Output**

- PXI-6040E, PXI-6070E, and PXI-6071E

These PXI E Series boards supply two channels of analog output voltage at the I/O connector. The reference and range for the analog output circuitry is software selectable. The reference can be either internal or external, whereas the range can be either bipolar or unipolar.
PXI-6030E and PXI-6031E

These boards supply two channels of analog output voltage at the I/O connector. The range is software-selectable between unipolar (0 to 10 V) and bipolar (±10 V).

**Analog Output Reference Selection**

PXI-6040E, PXI-6070E, and PXI-6071E

You can connect each D/A converter (DAC) to these PXI E Series boards’ internal reference of 10 V or to the external reference signal connected to the external reference (EXTREF) pin on the I/O connector. This signal applied to EXTREF should be within ±11 V. You do not need to configure both channels for the same mode.

**Analog Output Polarity Selection**

You can configure each analog output channel for either unipolar or bipolar output. A unipolar configuration has a range of 0 to $V_{ref}$ at the analog output. A bipolar configuration has a range of $-V_{ref}$ to $+V_{ref}$ at the analog output. $V_{ref}$ is the voltage reference used by the DACs in the analog output circuitry and can be either the +10 V onboard reference or an externally supplied reference within ±11 V. You do not need to configure both channels for the same range.

Selecting a bipolar range for a particular DAC means that any data written to that DAC will be interpreted as two’s complement format. In two’s complement mode, data values written to the analog output channel can be either positive or negative. If you select unipolar range, data is interpreted in straight binary format. In straight binary mode, data values written to the analog output channel range must be positive.

**Analog Output Reglitch Selection**

PXI-6070E and PXI-6071E

In normal operation, a DAC output will glitch whenever it is updated with a new value. The glitch energy differs from code to code and appears as distortion in the frequency spectrum. Each analog output contains a reglitch circuit that generates uniform glitch energy at every code rather than large glitches at the major code transitions. This uniform glitch energy appears as a multiple of the update rate in the frequency spectrum. Notice that this reglitch circuit does not eliminate the glitches; it only makes them more uniform in size. Reglitching is normally disabled at startup and your software can independently enable each channel.
Analog Trigger

In addition to supporting internal software triggering and external digital triggering to initiate a data acquisition sequence, these boards also support analog triggering. You can configure the analog trigger circuitry to accept either a direct analog input from the PFI0/TRIG1 pin on the I/O connector or a postgain signal from the output of the PGIA, as shown in Figure 3-4. The trigger-level range for the direct analog channel is ±10 V in 78 mV steps for the PXI-6040E, PXI-6070E, and PXI-6071E, and ±10 V in 4.9 mV steps for the PXI-6030E and PXI-6031E. The range for the post-PGIA trigger selection is simply the full-scale range of the selected channel, and the resolution is that range divided by 256 for the PXI-6040E, PXI-6070E, and PXI-6071E and divided by 4,096 for the PXI-6030E and PXI-6031E.

**Note** The PFI0/TRIG1 pin is an analog input when configured as an analog trigger. Therefore, it is susceptible to crosstalk from adjacent pins, which can result in false triggering when the pin is left unconnected. To avoid false triggering, make sure this pin is connected to a low-impedance signal source (less than 1 kΩ source impedance) if you plan to enable this input via software.

![Analog Trigger Block Diagram](image)

There are five analog triggering modes available, as shown in Figures 3-5 through 3-9. You can set lowValue and highValue independently in software.
In below-low-level analog triggering mode, the trigger is generated when the signal value is less than lowValue. HighValue is unused.

![Figure 3-5. Below-Low-Level Analog Triggering Mode](image1.png)

In above-high-level analog triggering mode, the trigger is generated when the signal value is greater than highValue. LowValue is unused.

![Figure 3-6. Above-High-Level Analog Triggering Mode](image2.png)

In inside-region analog triggering mode, the trigger is generated when the signal value is between the lowValue and the highValue.

![Figure 3-7. Inside-Region Analog Triggering Mode](image3.png)
In high-hysteresis analog triggering mode, the trigger is generated when the signal value is greater than $\text{highValue}$, with the hysteresis specified by $\text{lowValue}$.

![High-Hysteresis Analog Triggering Mode](image)

**Figure 3-8.** High-Hysteresis Analog Triggering Mode

In low-hysteresis analog triggering mode, the trigger is generated when the signal value is less than $\text{lowValue}$, with the hysteresis specified by $\text{highValue}$.

![Low-Hysteresis Analog Triggering Mode](image)

**Figure 3-9.** Low-Hysteresis Analog Triggering Mode

The analog trigger circuit generates an internal digital trigger based on the analog input signal and the user-defined trigger levels. This digital trigger can be used by any of the timing sections of the DAQ-STC, including the analog input, analog output, and general-purpose counter/timer sections. For example, the analog input section can be configured to acquire $n$ scans after the analog input signal crosses a specific threshold. As another example, the analog output section can be configured to update its outputs whenever the analog input signal crosses a specific threshold.
Digital I/O

The PXI E Series boards contain eight lines of digital I/O for general-purpose use. You can individually software-configure each line for either input or output. At system startup and reset, the digital I/O ports are all high impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the general-purpose counters. The up/down control signals are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC provides a very flexible interface for connecting timing signals to other boards or external circuitry. Your PXI E Series board uses the RTSI bus to interconnect timing signals between boards, and the Programmable Function Input (PFI) pins on the I/O connector to connect the board to external circuitry and other boards. These connections are designed to enable the PXI E Series board to both control and be controlled by other boards and circuits.

There are a total of 13 timing signals internal to the DAQ-STC that can be controlled by an external source. These timing signals can also be controlled by signals generated internally to the DAQ-STC, and these selections are fully software configurable. For example, the signal routing multiplexer for controlling the CONVERT* signal is shown in Figure 3-10.
Figure 3-10. CONVERT* Signal Routing

This figure shows that CONVERT* can be generated from a number of sources, including the external signals RTSI<0..6> and PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Many of these timing signals are also available as outputs on the RTSI pins, as indicated in the RTSI Triggers section later in this chapter, and on the PFI pins, as indicated in Chapter 4, Signal Connections.

Programmable Function Inputs

The 10 PFIs are connected to the signal routing multiplexer for each timing signal, and software can select one of the PFIs as the external source for a given timing signal. It is important to note that any of the PFIs can be used as an input by any of the timing signals and that multiple timing signals can use the same PFI simultaneously. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications. You can also individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software can turn on the output driver for the PFI5/UPDATE* pin.
Board and RTSI Clocks

Many functions performed by the PXI E Series boards require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector.

A PXI E Series board uses either its internal 20 MHz timebase or a timebase received over the RTSI bus. In addition, if you configure the board to use the internal timebase, you can also program the board to drive its internal timebase over the RTSI bus to another board that is programmed to receive this timebase signal. This clock source, whether local or from the RTSI bus, is used directly by the board as the primary frequency source. The default configuration at startup is to use the internal timebase without driving the RTSI bus timebase signal. This timebase is software selectable.

The RTSI Clock connects to other boards through the PXI Trigger bus on the PXI backplane. The RTSI Clock signal uses the PXI Trigger<7> line for this connection.

RTSI Triggers

The seven RTSI trigger lines on the RTSI bus provide a flexible interconnection scheme for any PXI E Series board sharing the RTSI bus. These bidirectional lines can drive any of eight timing signals onto the RTSI bus and can receive any of these timing signals. The RTSI trigger lines connect to other boards through the PXI bus on the PXI backplane. RTSI<0..5> connect to PXI Trigger<0..5>, respectively. RTSI<6> connects to PXI Star. This signal connection scheme is shown in Figure 3-11.
Chapter 3  Hardware Overview

Figure 3-11. RSTI Bus Signal Connection
This chapter describes how to make input and output signal connections to your PXI E Series board via the board I/O connector.

The I/O connector for the PXI-6030E, PXI-6040E, and PXI-6070E has 68 pins that you can connect to 68-pin accessories with the SH6868 shielded cable or the R6868 ribbon cable. With the SH6850 shielded cable or R6850 ribbon cable, you can connect your board to 50-pin signal conditioning modules and terminal blocks.

The I/O connector for the PXI-6031E and PXI-6071E has 100 pins that you can connect to 100-pin accessories with the SH100100 shielded cable. With the SH1006868 shielded cable you can connect your board to 68-pin accessories, and with the R1005050 ribbon cable you can connect your board to 50-pin accessories.

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector on the PXI-6030E, PXI-6040E, and PXI-6070E. Figure 4-2 shows the pin assignments for the 100-pin I/O connector on the PXI-6031E and PXI-6071E. Refer to Appendix B, Optional Cable Connector Descriptions, for the pin assignments for the 50-pin connector. A signal description follows the connector pin assignments.

Caution Connections that exceed any of the maximum ratings of input or output signals on the PXI E Series boards can damage the PXI E Series board and the computer. Maximum input ratings for each signal are given in the Protection column of Table 4-1. National Instruments is not liable for any damages resulting from such signal connections.
Figure 4-1. I/O Connector Pin Assignment for the PXI-6030E, PXI-6040E, and PXI-6070E
<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>AIGND</td>
<td>1</td>
<td>ACH16</td>
</tr>
<tr>
<td>AIGND</td>
<td>2</td>
<td>ACH24</td>
</tr>
<tr>
<td>ACH0</td>
<td>3</td>
<td>ACH17</td>
</tr>
<tr>
<td>ACH8</td>
<td>4</td>
<td>ACH25</td>
</tr>
<tr>
<td>ACH1</td>
<td>5</td>
<td>ACH18</td>
</tr>
<tr>
<td>ACH9</td>
<td>6</td>
<td>ACH26</td>
</tr>
<tr>
<td>ACH2</td>
<td>7</td>
<td>ACH19</td>
</tr>
<tr>
<td>ACH10</td>
<td>8</td>
<td>ACH27</td>
</tr>
<tr>
<td>ACH3</td>
<td>9</td>
<td>ACH20</td>
</tr>
<tr>
<td>ACH11</td>
<td>10</td>
<td>ACH28</td>
</tr>
<tr>
<td>ACH4</td>
<td>11</td>
<td>ACH21</td>
</tr>
<tr>
<td>ACH12</td>
<td>12</td>
<td>ACH29</td>
</tr>
<tr>
<td>ACH5</td>
<td>13</td>
<td>ACH32</td>
</tr>
<tr>
<td>ACH13</td>
<td>14</td>
<td>ACH30</td>
</tr>
<tr>
<td>ACH6</td>
<td>15</td>
<td>ACH33</td>
</tr>
<tr>
<td>ACH14</td>
<td>16</td>
<td>ACH31</td>
</tr>
<tr>
<td>ACH7</td>
<td>17</td>
<td>ACH32</td>
</tr>
<tr>
<td>ACH15</td>
<td>18</td>
<td>ACH40</td>
</tr>
<tr>
<td>AISENSE</td>
<td>19</td>
<td>ACH33</td>
</tr>
<tr>
<td>DACOUT</td>
<td>20</td>
<td>ACH41</td>
</tr>
<tr>
<td>DAC1OUT</td>
<td>21</td>
<td>ACH34</td>
</tr>
<tr>
<td>EXTREF</td>
<td>22</td>
<td>ACH42</td>
</tr>
<tr>
<td>AOIN0</td>
<td>23</td>
<td>ACH35</td>
</tr>
<tr>
<td>DO0</td>
<td>24</td>
<td>ACH43</td>
</tr>
<tr>
<td>DO4</td>
<td>25</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>DO1</td>
<td>26</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>DO2</td>
<td>27</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>DO5</td>
<td>28</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>DO2</td>
<td>29</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>DO6</td>
<td>30</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>DO3</td>
<td>31</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>DO7</td>
<td>32</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>DGD</td>
<td>33</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>+5 V</td>
<td>34</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>+5 V</td>
<td>35</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>SCANCLK</td>
<td>36</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>EXTSTROBE*</td>
<td>37</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>PFI0/GPI01</td>
<td>38</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>PFI1/GPI02</td>
<td>39</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>PFI2/CONVERT*</td>
<td>40</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>PFI3/GPI01_SOURCE</td>
<td>41</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>PFI4/GPI01_GATE</td>
<td>42</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>GPI01_OUTPUT</td>
<td>43</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>PFI0/GPI02_UPDATE*</td>
<td>44</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>PFI6/WFTRIG</td>
<td>45</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>PFI7/STARTSCAN</td>
<td>46</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>PFI8/GPI02_SOURCE</td>
<td>47</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>PFI9/GPI02_GATE</td>
<td>48</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>GPI02_OUTPUT</td>
<td>49</td>
<td>AISENSE2</td>
</tr>
<tr>
<td>FREQ_OUTPUT</td>
<td>50</td>
<td>AISENSE2</td>
</tr>
</tbody>
</table>

1 Not available on the PCI-6031E

Figure 4-2. I/O Connector Pin Assignment for the PXI-6031E and PXI-6071E
## I/O Connector Signal Descriptions

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Reference</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AIGND</td>
<td>—</td>
<td>—</td>
<td>Analog Input Ground—These pins are the reference point for single-ended measurements in RSE configuration and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected together on your PXI E Series board.</td>
</tr>
<tr>
<td>ACH&lt;0..15&gt;</td>
<td>AIGND</td>
<td>Input</td>
<td>Analog Input Channels 0 through 15—Each channel pair, ACH&lt;i, i+8&gt; (i = 0..7), can be configured as either one differential input or two single-ended inputs.</td>
</tr>
<tr>
<td>ACH&lt;16..63&gt;</td>
<td>AIGND</td>
<td>Input</td>
<td>Analog Input Channels 16 through 63 (PXI-6031E and PXI-6071E only)—Each channel pair, ACH&lt;i, i+8&gt; (i = 16..23, 32..39, 48..55), can be configured as either one differential input or two single-ended inputs.</td>
</tr>
<tr>
<td>AISENSE</td>
<td>AIGND</td>
<td>Input</td>
<td>Analog Input Sense—This pin serves as the reference node for any of channels ACH&lt;0..15&gt; in NRSE configuration.</td>
</tr>
<tr>
<td>AISENSE2</td>
<td>AIGND</td>
<td>Input</td>
<td>Analog Input Sense (PXI-6031E and PXI-6071E only)—This pin serves as the reference node for any of channels ACH&lt;16..63&gt; in NRSE configuration.</td>
</tr>
<tr>
<td>DAC0OUT</td>
<td>AOGND</td>
<td>Output</td>
<td>Analog Channel 0 Output—This pin supplies the voltage output of analog output channel 0.</td>
</tr>
<tr>
<td>DAC1OUT</td>
<td>AOGND</td>
<td>Output</td>
<td>Analog Channel 1 Output—This pin supplies the voltage output of analog output channel 1.</td>
</tr>
<tr>
<td>EXTREF</td>
<td>AOGND</td>
<td>Input</td>
<td>External Reference—This is the external reference input for the analog output circuitry. (This pin is not available on the PXI-6030E or PXI-6031E.)</td>
</tr>
<tr>
<td>AOGND</td>
<td>—</td>
<td>—</td>
<td>Analog Output Ground—The analog output voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected together on your PXI E Series board.</td>
</tr>
<tr>
<td>DGND</td>
<td>—</td>
<td>—</td>
<td>Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply. All three ground references—AIGND, AOGND, and DGND—are connected together on your PXI E Series board.</td>
</tr>
<tr>
<td>DIO&lt;0..7&gt;</td>
<td>DGND</td>
<td>Input or Output</td>
<td>Digital I/O signals—DIO6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.</td>
</tr>
<tr>
<td>+5 V</td>
<td>DGND</td>
<td>Output</td>
<td>+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-resetting.</td>
</tr>
<tr>
<td>SCANCLK</td>
<td>DGND</td>
<td>Output</td>
<td>Scan Clock—This pin pulses once for each A/D conversion in the scanning modes when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.</td>
</tr>
<tr>
<td>Signal Name</td>
<td>Reference</td>
<td>Direction</td>
<td>Description (Continued)</td>
</tr>
<tr>
<td>------------------</td>
<td>-----------</td>
<td>-----------</td>
<td>------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>EXTSTROBE*</td>
<td>DGND</td>
<td>Output</td>
<td>External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.</td>
</tr>
<tr>
<td>PFI0/TRIG1</td>
<td>DGND</td>
<td>Input</td>
<td>PFI0/Trigger 1—As an input, this is either one of the Programmable Function Inputs (PFIs) or the source for the hardware analog trigger. PFI signals are explained in the Timing Connections section later in this chapter. The hardware analog trigger is explained in the Analog Trigger section in Chapter 3, Hardware Overview. Analog trigger is available only on the PXI-6030E, PXI-6031E, PXI-6040E, PXI-6070E, and PXI-6071E. As an output, this is the TRIG1 signal. In posttrigger data acquisition sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.</td>
</tr>
<tr>
<td>PFI1/TRIG2</td>
<td>DGND</td>
<td>Input</td>
<td>PFI1/Trigger 2—As an input, this is one of the PFIs. As an output, this is the TRIG2 signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.</td>
</tr>
<tr>
<td>PFI2/CONVERT*</td>
<td>DGND</td>
<td>Input</td>
<td>PFI2/Convert—As an input, this is one of the PFIs. As an output, this is the CONVERT* signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.</td>
</tr>
<tr>
<td>PFI3/GPCTR1_SOURCE</td>
<td>DGND</td>
<td>Input</td>
<td>PFI3/Counter 1 Source—As an input, this is one of the PFIs. As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.</td>
</tr>
<tr>
<td>PFI4/GPCTR1_GATE</td>
<td>DGND</td>
<td>Input</td>
<td>PFI4/Counter 1 Gate—As an input, this is one of the PFIs. As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.</td>
</tr>
<tr>
<td>GPCTR1_OUT</td>
<td>DGND</td>
<td>Output</td>
<td>Counter 1 Output—This output is from the general-purpose counter 1 output.</td>
</tr>
<tr>
<td>PFI5/UPDATE*</td>
<td>DGND</td>
<td>Input</td>
<td>PFI5/Update—As an input, this is one of the PFIs. As an output, this is the UPDATE* signal. A high-to-low edge on UPDATE* indicates that the analog output primary group is being updated.</td>
</tr>
</tbody>
</table>
Table 4-1 shows the I/O signal summary for the PXI-6040E, PXI-6070E, and PXI-6071E.

### Table 4-1. I/O Signal Summary, PXI-6040E, PXI-6070E, and PXI-6071E

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Reference</th>
<th>Direction</th>
<th>Description (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PFI6/WFTRIG</td>
<td>DGND</td>
<td>Input</td>
<td>PFI6/Waveform Trigger—As an input, this is one of the PFI. As an output, this is the WFTRIG signal. In timed analog output sequences, a low-to-high transition indicates the initiation of the waveform generation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>PFI7/STARTSCAN</td>
<td>DGND</td>
<td>Input</td>
<td>PFI7/Start of Scan—As an input, this is one of the PFI. As an output, this is the STARTSCAN signal. This pin pulses once at the start of each analog input scan in the interval scan. A low-to-high transition indicates the start of the scan.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>PFI8/GPCTR0_SOURCE</td>
<td>DGND</td>
<td>Input</td>
<td>PFI8/Counter 0 Source—As an input, this is one of the PFI. As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>PFI9/GPCTR0_GATE</td>
<td>DGND</td>
<td>Input</td>
<td>PFI9/Counter 0 Gate—As an input, this is one of the PFI. As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>GPCTR0_OUT</td>
<td>DGND</td>
<td>Output</td>
<td>Counter 0 Output—This output is from the general-purpose counter 0 output.</td>
</tr>
<tr>
<td>FREQ_OUT</td>
<td>DGND</td>
<td>Output</td>
<td>Frequency Output—This output is from the frequency generator output.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Signal Type and Direction</th>
<th>Impedance</th>
<th>Protection (Volts)</th>
<th>Source (mA at V)</th>
<th>Sink (mA at V)</th>
<th>Rise Time (ns)</th>
<th>Bias</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACH&lt;0..63&gt;</td>
<td>AI</td>
<td>100 GΩ in parallel with 100 pF</td>
<td>25/15</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>±200 pA</td>
</tr>
<tr>
<td>(ACH&lt;16..63&gt; for PXI-6071E only)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AISENSE, AISENSE2</td>
<td>AI</td>
<td>100 GΩ in parallel with 100 pF</td>
<td>25/15</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>±200 pA</td>
</tr>
<tr>
<td>(AISENSE2 for PXI-6071E only)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AIGND</td>
<td>AO</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

---

**Note:** The table lists the signal names, their types, directions, and related descriptions. The impedance values are given in parallel with capacitive elements where applicable. The protection levels are specified in Volts (Volts) and are crucial for understanding the output levels. Source and sink values are also provided in milliamperes (mA) at a specific voltage (V).
### Table 4-1. I/O Signal Summary, PXI-6040E, PXI-6070E, and PXI-6071E (Continued)

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Signal Type and Direction</th>
<th>Impedance Input/Output</th>
<th>Protection (Volts) On/Off</th>
<th>Source (mA at V)</th>
<th>Sink (mA at V)</th>
<th>Rise Time (ns)</th>
<th>Bias</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC0OUT</td>
<td>AO</td>
<td>0.1 Ω</td>
<td>Short-circuit to ground</td>
<td>5 at 10</td>
<td>5 at -10</td>
<td>20 V/μs</td>
<td>—</td>
</tr>
<tr>
<td>DAC1OUT</td>
<td>AO</td>
<td>0.1 Ω</td>
<td>Short-circuit to ground</td>
<td>5 at 10</td>
<td>5 at -10</td>
<td>20 V/μs</td>
<td>—</td>
</tr>
<tr>
<td>EXTREF</td>
<td>AI</td>
<td>10 kΩ</td>
<td>25/15</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>AOGND</td>
<td>AO</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>DGND</td>
<td>DO</td>
<td>—</td>
<td>Short-circuit to ground</td>
<td>1A</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>VCC</td>
<td>DO</td>
<td>0.1 Ω</td>
<td>Short-circuit to ground</td>
<td>1A</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>DIO&lt;0..7&gt;</td>
<td>DIO</td>
<td>—</td>
<td></td>
<td>13 at (V_{cc} –0.4)</td>
<td>24 at 0.4</td>
<td>1.1</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>SCANCLK</td>
<td>DO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>EXTSTROBE*</td>
<td>DO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>PFI0/TRIG1</td>
<td>AI/DIO</td>
<td>10 kΩ</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>9 kΩ pu and 10 kΩ pd</td>
</tr>
<tr>
<td>PFI1/TRIG2</td>
<td>DIO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>PFI2/CONVERT*</td>
<td>DIO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>PFI3/GPCTR1_SOURCE</td>
<td>DIO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>PFI4/GPCTR1_GATE</td>
<td>DIO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>GPCTR1_OUT</td>
<td>DO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>PFI5/UPDATE*</td>
<td>DIO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>PFI6/WFTRIG</td>
<td>DIO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>PFI7/STARTSCAN</td>
<td>DIO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>PFI8/GPCTR0_SOURCE</td>
<td>DIO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>PFI9/GPCTR0_GATE</td>
<td>DIO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>GPCTR0_OUT</td>
<td>DO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>FREQ_OUT</td>
<td>DO</td>
<td>—</td>
<td></td>
<td>3.5 at (V_{cc} –0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
</tbody>
</table>

AI = Analog Input  DIO = Digital Input/Output  pu = pull-up  
AO = Analog Output  DO = Digital Output  AI/DIO = Analog/Digital Input/Output

**Note:** The tolerance on the 50 kΩ pullup and pulldown resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.
Table 4-2 shows the I/O signal summary for the PXI-6030E and PXI-6031E.

**Table 4-2. I/O Signal Summary, PXI-6030E and PXI-6031E**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Signal Type and Direction</th>
<th>Impedance Input/Output</th>
<th>Protection (Volts) On/Off</th>
<th>Source (mA at V)</th>
<th>Sink (mA at V)</th>
<th>Rise Time (ns)</th>
<th>Bias</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACH&lt;0..63&gt; (ACH&lt;16..63&gt; for PXI-6031E only)</td>
<td>AI</td>
<td>100 GΩ in parallel with 100 pF</td>
<td>25/15</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>±1 nA</td>
</tr>
<tr>
<td>AISENSE, AISENSE2 (AISENSE2 for PXI-6031E only)</td>
<td>AI</td>
<td>100 GΩ in parallel with 100 pF</td>
<td>25/15</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>±1 nA</td>
</tr>
<tr>
<td>AIGND</td>
<td>AO</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>DAC0OUT</td>
<td>AO</td>
<td>0.1 Ω</td>
<td>Short-circuit to ground</td>
<td>5 at 10</td>
<td>5 at -10</td>
<td>5 V/μs</td>
<td>—</td>
</tr>
<tr>
<td>DAC1OUT</td>
<td>AO</td>
<td>0.1 Ω</td>
<td>Short-circuit to ground</td>
<td>5 at 10</td>
<td>5 at -10</td>
<td>5 V/μs</td>
<td>—</td>
</tr>
<tr>
<td>AOGND</td>
<td>AO</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>DGND</td>
<td>DO</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>VCC</td>
<td>DO</td>
<td>0.1 Ω</td>
<td>Short-circuit to ground</td>
<td>1 A</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>DIO&lt;0..7&gt;</td>
<td>DIO</td>
<td>V_{cc} +0.5</td>
<td>13 at (V_{cc} -0.4)</td>
<td>24 at 0.4</td>
<td>1.1</td>
<td>50 kΩ pu</td>
<td></td>
</tr>
<tr>
<td>SCANCLK</td>
<td>DO</td>
<td>—</td>
<td>—</td>
<td>3.5 at (V_{cc} -0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>EXTSTOPROBE*</td>
<td>DO</td>
<td>—</td>
<td>—</td>
<td>3.5 at (V_{cc} -0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>PF10/TRIG1</td>
<td>AI</td>
<td>10 kΩ</td>
<td>±35 V_{cc} +0.5</td>
<td>3.5 at (V_{cc} -0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>9 kΩ pu and 10 kΩ pd</td>
</tr>
<tr>
<td>PF11/TRIG2</td>
<td>DIO</td>
<td>V_{cc} +0.5</td>
<td>3.5 at (V_{cc} -0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
<td></td>
</tr>
<tr>
<td>PF12/CONVERT*</td>
<td>DIO</td>
<td>V_{cc} +0.5</td>
<td>3.5 at (V_{cc} -0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
<td></td>
</tr>
<tr>
<td>PF13/GPCTR1_SOURCE</td>
<td>DIO</td>
<td>V_{cc} +0.5</td>
<td>3.5 at (V_{cc} -0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
<td></td>
</tr>
<tr>
<td>PF14/GPCTR1_GATE</td>
<td>DIO</td>
<td>V_{cc} +0.5</td>
<td>3.5 at (V_{cc} -0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
<td></td>
</tr>
<tr>
<td>GPCTR1_OUT</td>
<td>DO</td>
<td>—</td>
<td>—</td>
<td>3.5 at (V_{cc} -0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
</tr>
<tr>
<td>PF15/UPDATE*</td>
<td>DIO</td>
<td>V_{cc} +0.5</td>
<td>3.5 at (V_{cc} -0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
<td></td>
</tr>
<tr>
<td>PF16/WTTRIG</td>
<td>DIO</td>
<td>V_{cc} +0.5</td>
<td>3.5 at (V_{cc} -0.4)</td>
<td>5 at 0.4</td>
<td>1.5</td>
<td>50 kΩ pu</td>
<td></td>
</tr>
</tbody>
</table>
Analog Input Signal Connections

- **PXI-6030E, PXI-6040E, and PXI-6070E**
  
  The analog input signals for the PXI E Series boards are ACH<0..15>, AISENSE, and AIGND. The ACH<0..15> signals are tied to the 16 analog input channels of your PXI E Series board. In single-ended mode, signals connected to ACH<0..15> are routed to the positive input of the board PGIA. In differential mode, signals connected to ACH<0..7> are routed to the positive input of the PGIA, and signals connected to ACH<8..15> are routed to the negative input of the PGIA.

- **PXI-6031E and PXI-6071E**
  
  The analog input signals are ACH<0..63>, AISENSE, AISENSE2, and AIGND. The ACH<0..63> signals are tied to the 64 analog input channels of the boards. In single-ended mode, signals connected to ACH<0..31> are routed to the positive input of the PGIA. In differential mode, signals connected to ACH<0..7, 16..23, 32..39, 48..55> are routed to the positive input of the PGIA, and signals connected to ACH<8..15, 24..31, 40..47, 56..63> are routed to the negative input of the PGIA.

⚠ **Caution** Exceeding the differential and common-mode input ranges distorts your input signals. Exceeding the maximum input voltage rating can damage the PXI E Series board and the computer. National Instruments is not liable for any damages resulting from such signal connections. The maximum input voltage ratings are listed in the Protection column of Table 4-1.
In NRSE mode, the AISENSE (or AISENSE2 signal for the ACH<16..63>) signal is connected internally to the negative input of the PXI E Series board PGIA when their corresponding channels are selected. In DIFF and RSE modes, this signal is left unconnected.

AIGND is an analog input common signal that is routed directly to the ground tie point on the PXI E Series boards. You can use this signal for a general analog ground tie point to your PXI E Series board if necessary.

Connection of analog input signals to your PXI E Series board depends on the configuration of the analog input channels you are using and the type of input signal source. With the different configurations, you can use the PGIA in different ways. Figure 4-3 shows a diagram of your PXI E Series board PGIA.

![Diagram of PXI E Series PGIA](image)

The PGIA applies gain and common-mode voltage rejection and presents high input impedance to the analog input signals connected to your PXI E Series board. Signals are routed to the positive and negative inputs of the PGIA through input multiplexers on the board. The PGIA converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the ground for the board. Your PXI E Series board A/D converter (ADC) measures this output voltage when it performs A/D conversions.
You must reference all signals to ground either at the source device or at the board. If you have a floating source, you should reference the signal to ground by using the RSE input mode or the DIFF input configuration with bias resistors (see the Differential Connections for Nonreferenced or Floating Signal Sources section later in this chapter). If you have a grounded source, you should not reference the signal to AIGND. You can avoid this reference by using DIFF or NRSE input configurations.

Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground-referenced. The following sections describe these two types of signals.

Floating Signal Sources

A floating signal source is not connected in any way to the building ground system but, rather, has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must tie the ground reference of a floating signal to your PXI E Series board analog input ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

A ground-referenced signal source is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the PXI E Series board, assuming that the computer is plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are not properly connected. If a grounded signal source is improperly measured, this difference may appear as an error in the measurement. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.
Input Configurations

You can configure your PXI E Series board for one of three input modes—NRSE, RSE, or DIFF. The following sections discuss the use of single-ended and differential measurements and considerations for measuring both floating and ground-referenced signal sources.

Table 4-3 summarizes the recommended input configuration for both types of signal sources.
Table 4-3. Summary of Analog Input Connections

<table>
<thead>
<tr>
<th>DIFF Input Examples and Signal Source</th>
<th>Floating Signal Source (Not Connected to Building Ground)</th>
<th>Grounded Signal Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Examples</td>
<td>• Ungrounded Thermocouples</td>
<td>• Plug-in cards with nonisolated outputs</td>
</tr>
<tr>
<td></td>
<td>• Signal conditioning with isolated outputs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Battery devices</td>
<td></td>
</tr>
<tr>
<td>Differential (DIFF)</td>
<td><img src="image" alt="DIFF Circuit" /></td>
<td><img src="image" alt="DIFF Circuit" /></td>
</tr>
<tr>
<td>Single-Ended Ground Referenced (RSE)</td>
<td><img src="image" alt="RSE Circuit" /></td>
<td><img src="image" alt="RSE Circuit" /></td>
</tr>
<tr>
<td>Ground-loop losses, $V_g$, are added to measured signal.</td>
<td><img src="image" alt="NRSE Circuit" /></td>
<td><img src="image" alt="NRSE Circuit" /></td>
</tr>
<tr>
<td>Single-Ended Nonreferenced (NRSE)</td>
<td><img src="image" alt="NRSE Circuit" /></td>
<td><img src="image" alt="NRSE Circuit" /></td>
</tr>
<tr>
<td>See text for information on bias resistors.</td>
<td><img src="image" alt="NRSE Circuit" /></td>
<td><img src="image" alt="NRSE Circuit" /></td>
</tr>
</tbody>
</table>
Differential Connection Considerations (DIFF Input Configuration)

A differential connection is one in which the PXI E Series board analog input signal has its own reference signal or signal return path. These connections are available when the selected channel is configured in DIFF input mode. The input signal is tied to the positive input of the PGIA, and its reference signal, or return, is tied to the negative input of the PGIA.

When you configure a channel for differential input, each signal uses two multiplexer inputs—one for the signal and one for its reference signal. Therefore, with a differential configuration for every channel, up to eight analog input channels are available (up to 32 channels on the PXI-6031E and PXI-6071E).

You should use differential input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the PXI E Series board are greater than 10 ft (3 m).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce picked up noise and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.
Differential Connections for Ground-Referenced Signal Sources

Figure 4-4 shows how to connect a ground-referenced signal source to a channel on the PXI E Series board configured in DIFF input mode.

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the PXI E Series board ground, shown as $V_{\text{cm}}$ in Figure 4-4.
Differential Connections for Nonreferenced or Floating Signal Sources

Figure 4-5 shows how to connect a floating signal source to a channel on the PXI E Series board configured in DIFF input mode.

Figure 4-5. Differential Input Connections for Nonreferenced Signals

Figure 4-5 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is not likely to remain within the common-mode signal range of the PGIA, and the PGIA will saturate, causing erroneous readings. You must reference the source to AIGND. The easiest way is simply to connect the positive side of the signal to the positive input of the PGIA and connect the negative side of the signal to AIGND as well as to the negative input of the PGIA, without any resistors at all. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).
However, for larger source impedances, this connection leaves the differential signal path significantly out of balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, and the PGIA does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically coupled noise. Also, this configuration does not load down the source (other than the very high input impedance of the PGIA).

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 4-5. This fully-balanced configuration offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 k\(\Omega\) and each of the two resistors is 100 k\(\Omega\), the resistors load down the source with 200 k\(\Omega\) and produce a –1% gain error.

Both inputs of the PGIA require a DC path to ground in order for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AIGND. If the source has low impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 k\(\Omega\) to 1 M\(\Omega\)). In this case, you can tie the negative input directly to AIGND. If the source has high output impedance, you should balance the signal path as previously described using the same value resistor on both the positive and negative inputs; you should be aware that there is some gain error from loading down the source.

**Single-Ended Connection Considerations**

A single-ended connection is one in which the PXI E Series board analog input signal is referenced to a ground that can be shared with other input signals. The input signal is tied to the positive input of the PGIA, and the ground is tied to the negative input of the PGIA.

When every channel is configured for single-ended input, up to 16 analog input channels are available (up to 64 on the PXI-6031E and PXI-6071E).
You can use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high level (greater than 1 V).
- The leads connecting the signal to the PXI E Series board are less than 10 ft (3 m).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

You can software configure the PXI E Series board channels for two different types of single-ended connections—RSE configuration and NRSE configuration. The RSE configuration is used for floating signal sources; in this case, the PXI E Series board provides the reference ground point for the external signal. The NRSE input configuration is used for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point and the PXI E Series board should not supply one.

In single-ended configurations, more electrostatic and magnetic noise couples into the signal connections than in differential configurations. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.
Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 4-6 shows how to connect a floating signal source to a channel on the PXI E Series board configured for RSE mode.

![Figure 4-6. Single-Ended Input Connections for Nonreferenced or Floating Signals](image)

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

To measure a grounded signal source with a single-ended configuration, you must configure your PXI E Series board in the NRSE input configuration. The signal is then connected to the positive input of the PXI E Series PGIA, and the signal local ground reference is connected to the negative input of the PGIA. The ground point of the signal should, therefore, be connected to the AISENSE pin (AISENSE2 for ACH<16..63> on the PXI-6031E and PXI-6071E). Any potential difference between the PXI E Series ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the PGIA, and this difference is rejected by the amplifier. If the input circuitry of a PXI E Series board were referenced to ground, in this situation as in the RSE input configuration, this difference in ground potentials would appear as an error in the measured voltage.
Figure 4-7 shows how to connect a grounded signal source to a channel on the PXI E Series board configured for NRSE mode.

**Common-Mode Signal Rejection Considerations**

Figures 4-4 and 4-7 show connections for signal sources that are already referenced to some ground point with respect to the PXI E Series board. In these cases, the PGIA can reject any voltage caused by ground potential differences between the signal source and the board. In addition, with differential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the board. The PGIA can reject common-mode signals as long as $V_{\text{in}^+}$ and $V_{\text{in}^-}$ (input signals) are both within ±11 V of AIGND.

**Analog Output Signal Connections**

The analog output signals are DAC0OUT, DAC1OUT, EXTREF, and AOGND. (EXTREF is not available on the PXI-6030E or PXI-6031E.)

DAC0OUT is the voltage output signal for analog output channel 0.
DAC1OUT is the voltage output signal for analog output channel 1.
EXTREF is the external reference input for both analog output channels. You must configure each analog output channel individually for external reference selection in order for the signal applied at the external reference input to be used by that channel. If you do not specify an external reference, the channel will use the internal reference. Analog output configuration options are explained in the Analog Output section in Chapter 3, Hardware Overview. The following ranges and ratings apply to the EXTREF input:

- Usable input voltage range: ±11 V peak with respect to AOGND
- Absolute maximum ratings: ±15 V peak with respect to AOGND

AOGND is the ground reference signal for both analog output channels and the external reference signal.

Figure 4-8 shows how to make analog output connections and the external reference input connection to your PXI E Series board.

The external reference signal can be either a DC or an AC signal. The board multiplies this reference signal by the DAC code (divided by the full-scale DAC code) to generate the output voltage.
Digital I/O Signal Connections

The digital I/O signals are DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground reference signal for the DIO port. You can program all lines individually to be inputs or outputs.

**Caution**  
*Exceeding the maximum input voltage ratings, which are listed in Table 4-1 can damage the PXI E Series board and the computer. National Instruments is not liable for any damages resulting from such signal connections.*

Figure 4-9 shows signal connections for three typical digital I/O applications.
Figure 4-9 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states such as the state of the switch shown in the figure. Digital output applications include sending TTL signals and driving external devices such as the LED shown in the figure.

### Power Connections

Two pins on the I/O connector supply +5 V from the computer power supply via a self-resetting fuse. The fuse will reset automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry.

- **Power rating** +4.65 to +5.25 VDC at 1 A

⚠️ **Caution** *Under no circumstances should you connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the PXI E Series board or any other device. Doing so can damage the PXI E Series board and the computer. National Instruments is not liable for damages resulting from such a connection.*

### Timing Connections

⚠️ **Caution** *Exceeding the maximum input voltage ratings, which are listed in Table 4-1 can damage the PXI E Series board and the computer. National Instruments is not liable for any damages resulting from such signal connections.*

All external control over the timing of your PXI E Series board is routed through the 10 programmable function inputs labeled PFI0 through PFI9. These signals are explained in detail in the next section, *Programmable Function Input Connections*. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many DAQ, waveform generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control any DAQ, waveform generation, and general-purpose timing signals.

The DAQ signals are explained in the *DAQ Timing Connections* section later in this chapter. The waveform generation signals are explained in the *Waveform Generation Timing Connections* section later in this chapter. The general-purpose timing signals are explained in the *General-Purpose Timing Signal Connections* section later in this chapter.
All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-10, which shows how to connect an external TRIG1 source and an external CONVERT* source to two PXI E Series board PFI pins.

**Figure 4-10.** Timing I/O Connections

**Programmable Function Input Connections**

There are a total of 13 internal timing signals that you can externally control from the PFI pins. The source for each of these signals is software-selectable from any of the PFIs when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the board I/O connector for different applications requiring alternative wiring.

You can individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the CONVERT* signal as an output on the I/O connector, software can turn on the output driver for the PFI2/CONVERT* pin. Be careful not to drive a PFI signal externally when it is configured as an output.
As an input, you can individually configure each PFI for edge or level detection and for polarity selection, as well. You can use the polarity selection for any of the 13 timing signals, but the edge or level detection will depend upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that individual signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse-width requirement in edge-detect mode.

In level-detection mode, there are no minimum or maximum pulse-width requirements imposed by the PFIs themselves, but there may be limits imposed by the particular timing signal being controlled. These requirements are listed later in this chapter.

**DAQ Timing Connections**

The DAQ timing signals are SCANCLK, EXTSTROBE*, TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, and SISOURCE.

Posttriggered data acquisition allows you to view only data that is acquired after a trigger event is received. A typical posttriggered DAQ sequence is shown in Figure 4-11. Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-12 shows a typical pretriggered DAQ sequence. The description for each signal shown in these figures is included later in this chapter.

![Figure 4-11. Typical Posttriggered Acquisition](image-url)
SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software-selectable but is typically configured so that a low-to-high leading edge can clock external analog input multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software enabled. Figure 4-13 shows the timing for the SCANCLK signal.

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of the EXTSTROBE* signal. A 10 µs and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode. Figure 4-14 shows the timing for the hardware-strobe mode EXTSTROBE* signal.
TRIG1 Signal

Any PFI pin can externally input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin.

Refer to Figures 4-11 and 4-12 for the relationship of TRIG1 to the DAQ sequence.

As an input, the TRIG1 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG1 signal starts the data acquisition sequence for both posttriggered and pretriggered acquisitions. The PXI-6030E, PXI-6031E, PXI-6040E, PXI-6070E, and PXI-6071E support analog triggering on the PFI0/TRIG1 pin. See Chapter 3, Hardware Overview, for more information on analog triggering.

As an output, the TRIG1 signal reflects the action that initiates a DAQ sequence. This is true even if the acquisition is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-15 and 4-16 show the input and output timing requirements for the TRIG1 signal.

![Figure 4-14. EXTSTROBE* Signal Timing](image)

![Figure 4-15. TRIG1 Input Signal Timing](image)
The board also uses the TRIG1 signal to initiate pretriggered DAQ operations. In most pretriggered applications, the TRIG1 signal is generated by a software trigger. Refer to the TRIG2 signal description for a complete description of the use of TRIG1 and TRIG2 in a pretriggered DAQ operation.

**TRIG2 Signal**

Any PFI pin can externally input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin.

Refer to Figure 4-12 for the relationship of TRIG2 to the DAQ sequence.

As an input, the TRIG2 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG2 signal initiates the posttriggered phase of a pretriggered acquisition sequence. In pretriggered mode, the TRIG1 signal initiates the data acquisition. The scan counter indicates the minimum number of scans before TRIG2 can be recognized. After the scan counter decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The board ignores the TRIG2 signal if it is asserted prior to the scan counter decrementing to zero. After the selected edge of TRIG2 is received, the board will acquire a fixed number of scans and the acquisition will stop. This mode acquires data both before and after receiving TRIG2.

As an output, the TRIG2 signal reflects the posttrigger in a pretriggered acquisition sequence. This is true even if the acquisition is being externally triggered by another PFI. The TRIG2 signal is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.
Figures 4-17 and 4-18 show the input and output timing requirements for the TRIG2 signal.

**STARTSCAN Signal**

Any PFI pin can externally input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin.

Refer to Figures 4-11 and 4-12 for the relationship of STARTSCAN to the DAQ sequence.

As an input, the STARTSCAN signal is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of the STARTSCAN signal initiates a scan. The sample interval counter starts if you select internally triggered CONVERT*.

As an output, the STARTSCAN signal reflects the actual start pulse that initiates a scan. This is true even if the starts are being externally triggered by another PFI. You have two output options. The first is an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the...
scan. The second action is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN will be deasserted \( t_{\text{off}} \) after the last conversion in the scan is initiated. This output is set to tri-state at startup.

Figures 4-19 and 4-20 show the input and output timing requirements for the STARTSCAN signal.

**Figure 4-19.** STARTSCAN Input Signal Timing

![STARTSCAN Input Signal Timing Diagram](image1)

**Figure 4-20.** STARTSCAN Output Signal Timing

![STARTSCAN Output Signal Timing Diagram](image2)
The CONVERT* pulses are masked off until the board generates the STARTSCAN signal. If you are using internally generated conversions, the first CONVERT* appears when the onboard sample interval counter reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN generates a conversion. The STARTSCAN pulses should be separated by at least one scan period.

A counter on your PXI E Series board internally generates the STARTSCAN signal unless you select some external source. This counter is started by the TRIG1 signal and is stopped either by software or by the sample counter.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

**CONVERT* Signal**

Any PFI pin can externally input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-11 and 4-12 for the relationship of CONVERT* to the DAQ sequence.

As an input, the CONVERT* signal is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of the CONVERT* signal initiates an A/D conversion.

As an output, the CONVERT* signal reflects the actual convert pulse that is connected to the ADC. This is true even if the conversions are being externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.
Figures 4-21 and 4-22 show the input and output timing requirements for the CONVERT* signal.

The ADC switches to hold mode within 60 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next. Separate the CONVERT* pulses by at least one conversion period.
The sample interval counter on the PXI E Series board normally generates the CONVERT* signal unless you select some external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan is finished. It then reloads itself in preparation for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

**AIGATE Signal**

Any PFI pin can externally input the AIGATE signal, which is not available as an output on the I/O connector. The AIGATE signal can mask off scans in a DAQ sequence. You can configure the PFI pin you select as the source for the AIGATE signal in either the level-detection or edge-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

In the level-detection mode if AIGATE is active, the STARTSCAN signal is masked off and no scans can occur. In the edge-detection mode, the first active edge disables the STARTSCAN signal, and the second active edge enables STARTSCAN.

The AIGATE signal can neither stop a scan in progress nor continue a previously gated-off scan; in other words, once a scan has started, AIGATE does not gate off conversions until the beginning of the next scan and, conversely, if conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

**SISOURCE Signal**

Any PFI pin can externally input the SISOURCE signal, which is not available as an output on the I/O connector. The onboard scan interval counter uses the SISOURCE signal as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for the SISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.
Either the 20 MHz or 100 kHz internal timebase generates the SISOURCE signal unless you select some external source. Figure 4-23 shows the timing requirements for the SISOURCE signal.

![Figure 4-23. SISOURCE Signal Timing](image)

**Waveform Generation Timing Connections**

The analog group defined for your PXI E Series board is controlled by WFTRIG, UPDATE*, and UISOURCE.

**WFTRIG Signal**

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, the WFTRIG signal is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of the WFTRIG signal starts the waveform generation for the DACs. The update interval (UI) counter is started if you select internally generated UPDATE*.

As an output, the WFTRIG signal reflects the trigger that initiates waveform generation. This is true even if the waveform generation is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.
Figures 4-24 and 4-25 show the input and output timing requirements for the WFTRIG signal.

**UPDATE* Signal**

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, the UPDATE* signal is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of the UPDATE* signal updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, the UPDATE* signal reflects the actual update pulse that is connected to the DACs. This is true even if the updates are being externally generated by another PFI. The output is an active low pulse with a pulse width of 100 to 150 ns. This output is set to tri-state at startup.
Figures 4-26 and 4-27 show the input and output timing requirements for the UPDATE* signal.

![UPDATE* Input Signal Timing](image)

**Figure 4-26. UPDATE* Input Signal Timing**

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

![UPDATE* Output Signal Timing](image)

**Figure 4-27. UPDATE* Output Signal Timing**

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The PXI E Series board UI counter normally generates the UPDATE* signal unless you select some external source. The UI counter is started by the WFTRIG signal and can be stopped by software or the internal Buffer Counter.

D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

**UISOURCE Signal**

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. The UI counter uses the UISOURCE signal as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for the UISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low. Figure 4-28 shows the timing requirements for the UISOURCE signal.
The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase normally generates the UISOURCE signal unless you select some external source.

**General-Purpose Timing Signal Connections**

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

**GPCTR0_SOURCE Signal**

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, the GPCTR0_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR0_SOURCE signal reflects the actual clock connected to general-purpose counter 0. This is true even if another PFI is externally inputting the source clock. This output is set to tri-state at startup.
Figure 4-29 shows the timing requirements for the GPCTR0_SOURCE signal.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR0_SOURCE signal unless you select some external source.

**GPCTR0_GATE Signal**

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, the GPCTR0_GATE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform actions such as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR0_GATE signal reflects the actual gate signal connected to general-purpose counter 0. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup.
Figure 4-30 shows the timing requirements for the GPCTR0_GATE signal.

![GPCTR0_GATE Signal Timing in Edge-Detection Mode](image)

**GPCTR0_OUT Signal**

This signal is available only as an output on the GPCTR0_OUT pin. The GPCTR0_OUT signal reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to tri-state at startup. Figure 4-31 shows the timing of the GPCTR0_OUT signal.

![GPCTR0_OUT Signal Timing](image)

**GPCTR0_UP_DOWN Signal**

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 will count down when this pin is at a logic low and count up when it is at a logic high. You can disable this input so that software can control the up-down functionality and leave the DIO6 pin free for general use.
**GPCTR1_SOURCE Signal**

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, the GPCTR1_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1. This is true even if the source clock is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-32 shows the timing requirements for the GPCTR1_SOURCE signal.

![Figure 4-32. GPCTR1_SOURCE Signal Timing](image)

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR1_SOURCE unless you select some external source.

**GPCTR1_GATE Signal**

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, the GPCTR1_GATE signal is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform such actions as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.
As an output, the GPCTR1_GATE signal monitors the actual gate signal connected to general-purpose counter 1. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-33 shows the timing requirements for the GPCTR1_GATE signal.

![Figure 4-33. GPCTR1_GATE Signal Timing in Edge-Detection Mode](image)

**GPCTR1_OUT Signal**

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC board general-purpose counter 1. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to tri-state at startup. Figure 4-34 shows the timing requirements for the GPCTR1_OUT signal.

![Figure 4-34. GPCTR1_OUT Signal Timing](image)

**GPCTR1_UP_DOWN Signal**

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that software can control the up-down functionality and
leave the DIO7 pin free for general use. Figure 4-35 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals of your PXI E Series board.

![GPCTR Timing Summary](image)

**Figure 4-35. GPCTR Timing Summary**

The GATE and OUT signal transitions shown in Figure 4-35 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, would apply when the counter is programmed to count falling edges.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on your PXI E Series board. Figure 4-35 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by \( t_{gsu} \) and \( t_{gh} \) in Figure 4-35. The gate signal is not required to be held after the active edge of the source signal.

If you use an internal timebase clock, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source
edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the PXI E Series boards. Figure 4-35 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

**FREQ_OUT Signal**

This signal is available only as an output on the FREQ_OUT pin. The PXI E Series board frequency generator outputs the FREQ_OUT pin. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software-selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software selectable. This output is set to tri-state at startup.

**Field Wiring Considerations**

Environmental noise can seriously affect the accuracy of measurements made with your PXI E Series board if you do not take proper care when running signal wires between signal sources and the board. The following recommendations apply mainly to analog input signal routing to the board, although they also apply to signal routing in general.

Minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential analog input connections to reject common-mode noise.

- Use individually shielded, twisted-pair wires to connect analog input signals to the board. With this type of wire, the signals attached to the ACH+ and ACH- inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.

- Route signals to the board carefully. Keep cabling away from noise sources. The most common noise source in a PXI data acquisition system is the video monitor. Separate the monitor from the analog signals as much as possible.
The following recommendations apply for all signal connections to your PXI E Series board:

- Separate PXI E Series board signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the PXI E Series board signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.

- Do not run signal lines through conduits that also contain power lines.

- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

For more information, refer to the application note, *Field Wiring and Noise Consideration for Analog Signals*, available from National Instruments.
This chapter discusses the calibration procedures for your PXI E Series board. If you are using the NI-DAQ device driver, that software includes calibration functions for performing all of the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the PXI E Series boards, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of board calibration is required for all but the most forgiving applications. If you do not calibrate your board, your signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you and described in this chapter. The first level is the fastest, easiest, and least accurate, whereas the last level is the slowest, most difficult, and most accurate.

**Loading Calibration Constants**

Your PXI E Series board is factory calibrated before shipment at approximately 25°C to the levels indicated in Appendix A, Specifications. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the board is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ software determines when this is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

In the EEPROM there is a user-modifiable calibration area in addition to the permanent factory calibration area. This means that you can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.
This method of calibration is not very accurate because it does not take into account the fact that the board measurement and output voltage errors can vary with time and temperature. It is better to self-calibrate when the board is installed in the environment in which it will be used.

### Self-Calibration

Your PXI E Series board can measure and correct for almost all of its calibration-related errors without any external signal connections. Your National Instruments software provides a self-calibration method. This self-calibration process, which generally takes less than a minute, is the preferred method of assuring accuracy in your application. Initiate self-calibration to minimize the effects of any offset, gain, and linearity drifts, particularly those due to warmup.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the following section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

### External Calibration

Your PXI E Series board has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, Specifications. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using your board at an extreme temperature or if the onboard reference has not been measured for a year or more, you may wish to externally calibrate your board.

An external calibration refers to calibrating your board with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process and the results can be saved in the EEPROM, so you should not have to perform an external calibration very often. You can externally calibrate your board by calling the NI-DAQ calibration function.

To externally calibrate your board, be sure to use a very accurate external reference. The reference should be several times more accurate than the board itself. For example, to calibrate a 16-bit board, the external reference should be at least ±0.001% (±10 ppm) accurate.
Other Considerations

The CalDACs adjust the gain error of each analog output channel by adjusting the value of the reference voltage supplied to that channel. This calibration mechanism is designed to work only with the internal 10 V reference. Thus, in general, it is not possible to calibrate the analog output gain error when using an external reference. In this case, it is advisable to account for the nominal gain error of the analog output channel either in software or with external hardware. See Appendix A, Specifications, for analog output gain error information.
Specifications

This appendix lists the specifications of each PXI E Series board. These specifications are typical at 25° C unless otherwise noted.

**PXI-6040E, PXI-6070E, and PXI-6071E**

**Analog Input**

**Input Characteristics**

Number of channels

- PXI-6040E and PXI-6070E ............ 16 single-ended, or 8 differential (software-selectable per channel)
- PXI-6071E ...................................... 64 single-ended or 32 differential (software-selectable per channel)

Type of ADC.......................................... Successive approximation

Resolution .............................................. 12 bits, 1 in 4,096

Maximum sampling rate (single-channel)\(^1\)

- PXI-6070E and PXI-6071E ............ 1.25 MS/s
- PXI-6040E ...................................... 500 kS/s

---

\(^1\) See settling time table in *Dynamic Characteristics* for multi-channel rates.
Input signal ranges

<table>
<thead>
<tr>
<th>Channel Gain (Software-Selectable)</th>
<th>Board Range (Software-Selectable)</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>±10 V</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>±5 V</td>
<td>0 to 10 V</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>±2.5 V</td>
<td>0 to 5 V</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>±1 V</td>
<td>0 to 2 V</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>±500 mV</td>
<td>0 to 1 V</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>±250 mV</td>
<td>0 to 500 mV</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>±100 mV</td>
<td>0 to 200 mV</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>±50 mV</td>
<td>0 to 100 mV</td>
<td></td>
</tr>
</tbody>
</table>

Input coupling.................................DC

Maximum working voltage (signal and common mode)....................Each input should remain within ±11 V of ground

Overvoltage protection.........................±25 V powered on, ±15 V powered off

Inputs protected
PXI-6040E and PXI-6070E.......................ACH<0..15>, AISENSE
PXI-6071E....................................ACH<0..63>, AISENSE, AISENSE2

FIFO buffer size..............................512 S

Data transfers..................................DMA, interrupts, programmed I/O

DMA modes.....................................Scatter-gather

Configuration memory size...............512 words

**Accuracy Information**

See following tables
# PXI-6040E Accuracy Information

<table>
<thead>
<tr>
<th>Nominal Range (V)</th>
<th>Absolute Accuracy</th>
<th>Relative Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>% of Reading</td>
<td>Offset</td>
</tr>
<tr>
<td>Positive FS</td>
<td>24 Hours</td>
<td>90 Days</td>
</tr>
<tr>
<td>10 -10</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>5 -5</td>
<td>0.0272%</td>
<td>0.0292%</td>
</tr>
<tr>
<td>2.5 -2.5</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>1 -1</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.5 -0.5</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.25 -0.25</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.1 -0.1</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.05 -0.05</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>10 0</td>
<td>0.0272%</td>
<td>0.0292%</td>
</tr>
<tr>
<td>5 0</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>2 0</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>1 0</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.5 0</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.2 0</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.1 0</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
</tbody>
</table>

Absolute Accuracy = (% of Reading × Voltage) + Offset + Noise + (Temp Drift × Voltage).

Note: Temp Drift applies only if ambient is greater than ±10° C of previous external calibration.

Accuracies are valid for measurements following an internal E Series Calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings.

Measurement accuracies are listed for operational temperatures within ±1° C of internal calibration temperature and ±10° C of external or factory calibration temperature.
## PXI-6070E and PXI-6071E Accuracy Information

<table>
<thead>
<tr>
<th>Nominal Range (V)</th>
<th>Absolute Accuracy</th>
<th>Relative Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>% of Reading</td>
<td>Offset</td>
</tr>
<tr>
<td>Positive FS</td>
<td>24 Hours</td>
<td>90 Days</td>
</tr>
<tr>
<td>10</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>5</td>
<td>0.0272%</td>
<td>0.0292%</td>
</tr>
<tr>
<td>2.5</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>1</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.5</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.25</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.1</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.05</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>10</td>
<td>0.0272%</td>
<td>0.0292%</td>
</tr>
<tr>
<td>5</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>2</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>1</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.5</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.2</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
<tr>
<td>0.1</td>
<td>0.0522%</td>
<td>0.0542%</td>
</tr>
</tbody>
</table>

Absolute Accuracy = (% of Reading × Voltage) + Offset + Noise + (Temp Drift × Voltage).

Note: Temp Drift applies only if ambient is greater than ±10° C of previous external calibration.

Accuracies are valid for measurements following an internal E Series Calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings.

Measurement accuracies are listed for operational temperatures within ±1° C of internal calibration temperature and ±10° C of external or factory calibration temperature.
Transfer Characteristics

Relative accuracy ................................... ±0.5 LSB typ dithered,
                   ±1.5 LSB max undithered

DNL ................................................. ±0.5 LSB typ, ±1 LSB max

No missing codes ......................... 12 bits, guaranteed

Offset error

<table>
<thead>
<tr>
<th>State</th>
<th>PXI-6070E and PXI-6071E</th>
<th>PXI-6040E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pregain error after calibration</td>
<td>±12 µV max</td>
<td>±16 µV max</td>
</tr>
<tr>
<td>Pregain error before calibration</td>
<td>±2.5 mV max</td>
<td>±4.0 mV max</td>
</tr>
<tr>
<td>Postgain error after calibration</td>
<td>±0.5 mV max</td>
<td>±0.8 mV max</td>
</tr>
<tr>
<td>Postgain error before calibration</td>
<td>±100 mV max</td>
<td>±200 mV max</td>
</tr>
</tbody>
</table>

Gain error (relative to calibration reference)

   After calibration (gain = 1) .......... ±0.02% of reading max
   Before calibration ................... ±2.5% of reading max
   Gain ≠ 1 with gain error
       adjusted to 0 at gain = 1 .......... ±0.02% of reading max

Amplifier Characteristics

Input impedance

   Normal powered on .................... 100 GΩ in parallel with 100 pF
   Powered off ........................... 820 Ω min.
   Overload .............................. 820 Ω min.

Input bias current ......................... ±200 pA

Input offset current ..................... ±100 pA
Appendix A Specifications for PXI-6040E, PXI-6070E, and PXI-6071E

CMRR, all input ranges, DC to 60 Hz

<table>
<thead>
<tr>
<th>Gain</th>
<th>PXI-6070E and PXI-6071E</th>
<th>PXI-6040E</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>95 dB</td>
<td>90 dB</td>
</tr>
<tr>
<td>1</td>
<td>100 dB</td>
<td>95 dB</td>
</tr>
<tr>
<td>≥2</td>
<td>106 dB</td>
<td>100 dB</td>
</tr>
</tbody>
</table>

Dynamic Characteristics

Bandwidth

<table>
<thead>
<tr>
<th>Board</th>
<th>Small Signal (–3 dB)</th>
<th>Large Signal (1% THD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PXI-6070E, PXI-6071E</td>
<td>1.6 MHz</td>
<td>1 MHz</td>
</tr>
<tr>
<td>PXI-6040E</td>
<td>600 kHz</td>
<td>350 kHz</td>
</tr>
</tbody>
</table>

Settling time to full-scale step

<table>
<thead>
<tr>
<th>Board</th>
<th>Gain</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>±0.012% (±0.5 LSB)</td>
</tr>
<tr>
<td>PXI-6070E</td>
<td>0.5</td>
<td>2 μS typ, 3 μS max</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>2 μS typ, 3 μS max</td>
</tr>
<tr>
<td></td>
<td>2 to 50</td>
<td>2 μS typ, 3 μS max</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>2 μS typ, 3 μS max</td>
</tr>
<tr>
<td>PXI-6040E</td>
<td>All</td>
<td>4 μS typ, 8 μS max</td>
</tr>
</tbody>
</table>
### System noise (LSB\textsubscript{rms}, not including quantization)

<table>
<thead>
<tr>
<th>Board</th>
<th>Gain</th>
<th>0.5 to 10</th>
<th>20</th>
<th>50</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>PXI-6070E, PXI-6071E</td>
<td>0.5</td>
<td>0.25</td>
<td>0.4</td>
<td>0.5</td>
<td>0.8</td>
</tr>
<tr>
<td>PXI-6070E, PXI-6071E</td>
<td>20</td>
<td>0.45</td>
<td>0.5</td>
<td>0.7</td>
<td>0.9</td>
</tr>
<tr>
<td>PXI-6070E, PXI-6071E</td>
<td>50</td>
<td>0.5</td>
<td>0.8</td>
<td>0.9</td>
<td>1.5</td>
</tr>
<tr>
<td>PXI-6070E, PXI-6071E</td>
<td>100</td>
<td>0.8</td>
<td>0.9</td>
<td>0.9</td>
<td>1.5</td>
</tr>
<tr>
<td>PXI-6040E</td>
<td>0.5</td>
<td>0.15</td>
<td>0.2</td>
<td>0.35</td>
<td>0.6</td>
</tr>
<tr>
<td>PXI-6040E</td>
<td>10 to 20</td>
<td>0.2</td>
<td>0.35</td>
<td>0.6</td>
<td>0.8</td>
</tr>
<tr>
<td>PXI-6040E</td>
<td>50</td>
<td>0.35</td>
<td>0.6</td>
<td>0.8</td>
<td>1.5</td>
</tr>
<tr>
<td>PXI-6040E</td>
<td>100</td>
<td>0.6</td>
<td>0.8</td>
<td>0.8</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Crosstalk......................................................... –80 dB, DC to 100 kHz

### Stability

**Offset temperature coefficient**

- Pregain...................................... ±5 \(\mu\text{V/°C}\)
- Postgain.................................... ±240 \(\mu\text{V/°C}\)

**Gain temperature coefficient............... ±20 ppm/°C**
Analog Output

Output Characteristics

Number of channels .................................................. 2 voltage
Resolution ....................................................................... 12 bits, 1 in 4,096

Max update rate
1 channel .......................................................... 1 MS/s
2 channel .......................................................... 600 kS/s–1 MS/s per channel (system-dependent)

Type of DAC ........................................................... Double-buffered, multiplying

FIFO buffer size
PXI-6070E, PXI-6071E ....................................... 2,048 S
PXI-6040E .......................................................... 512 S

Data transfers ............................................................. DMA, interrupts, programmed I/O

DMA modes ............................................................ Scatter gather

PXI-6040E Accuracy Information

<table>
<thead>
<tr>
<th>Nominal Range (V)</th>
<th>Positive FS</th>
<th>Negative FS</th>
<th>24 Hours</th>
<th>90 Days</th>
<th>1 Year</th>
<th>Offset</th>
<th>Temp Drift</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive FS</td>
<td>10</td>
<td>–10</td>
<td>0.0177%</td>
<td>0.0197%</td>
<td>0.0219%</td>
<td>±5.933 mV</td>
<td>0.0005%</td>
</tr>
<tr>
<td>Negative FS</td>
<td>10</td>
<td>0</td>
<td>0.0177%</td>
<td>0.0197%</td>
<td>0.0219%</td>
<td>±3.491 mV</td>
<td>0.0005%</td>
</tr>
</tbody>
</table>

Absolute Accuracy = (% of Reading × Voltage) + Offset + (Temp Drift × Voltage).

Note: Temp drift applies only if ambient is greater than ±10° C of previous external calibration.
Appendix A  Specifications for PXI-6040E, PXI-6070E, and PXI-6071E

PXI-6070E and PXI-6071E Accuracy Information

<table>
<thead>
<tr>
<th>Nominal Range (V)</th>
<th>Absolute Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>% of Reading</td>
</tr>
<tr>
<td>Positive FS</td>
<td>Negative FS</td>
</tr>
<tr>
<td>10</td>
<td>–10</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
</tr>
</tbody>
</table>

Absolute Accuracy = (% of Reading × Voltage) + Offset + (Temp Drift × Voltage).

Note: Temp drift applies only if ambient is greater than ±10° C of previous external calibration.

Transfer Characteristics

Relative accuracy (INL)

After calibration ...................... ±0.3 LSB typ, ±0.5 LSB max
Before calibration ..................... ±4 LSB max

DNL

After calibration ...................... ±0.3 LSB typ, ±1.0 LSB max
Before calibration ..................... ±3 LSB max

Monotonicity .............................. 12 bits, guaranteed after calibration

Offset error

After calibration ...................... ±1.0 mV max
Before calibration ..................... ±200 mV max

Gain error (relative to internal reference)

After calibration ...................... ±0.01% of output max
Before calibration ..................... ±0.5% of output max

Gain error (relative to external reference) ...................... +0% to +0.5% of output max, not adjustable

Voltage Output

Ranges .................................................... ±10 V, 0 to 10 V,
±EXTREF, 0 to EXTREF (software selectable)
Appendix A Specifications for PXI-6040E, PXI-6070E, and PXI-6071E

Output coupling ......................... DC
Output impedance ....................... 0.1 Ω max
Current drive .............................. ±5 mA max
Protection ............................... Short-circuit to ground
Power-on state ......................... 0 V

External reference input
  Range ...................................... ±11 V
  Overvoltage protection ............ ±25 V powered on,
  ............................................ ±15 V powered off
  Input impedance ..................... 10 kΩ
  Bandwidth (–3 dB) ................. 1 MHz

Dynamic Characteristics
Settling time for full-scale step .... 3 µs to ±0.5 LSB accuracy
Slew rate .................................. 20 V/µs
Noise ........................................ 200 µV rms, DC to 1 MHz
Glitch energy (at midscale transition)
  Magnitude
    Reglitching disabled ............ ±20 mV
    Reglitching enabled .......... ±4 mV
  Duration ................................ 1.5 µs

Stability
Offset temperature coefficient .... ±50 µV/° C
Gain temperature coefficient
  Internal reference ..................... ±25 ppm/° C
  External reference .................... ±25 ppm/° C

Digital I/O
Number of channels ..................... 8 input/output
Compatibility ........................... TTL/CMOS
Digital logic levels

<table>
<thead>
<tr>
<th>Level</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input low voltage</td>
<td>0.0 V</td>
<td>0.8 V</td>
</tr>
<tr>
<td>Input high voltage</td>
<td>2.0 V</td>
<td>5.0 V</td>
</tr>
<tr>
<td>Input low current ($V_{\text{in}} = 0 , \text{V}$)</td>
<td>—</td>
<td>—320 $\mu$A</td>
</tr>
<tr>
<td>Input high current ($V_{\text{in}} = 5 , \text{V}$)</td>
<td>—</td>
<td>10 $\mu$A</td>
</tr>
<tr>
<td>Output low voltage ($I_{\text{OL}} = 24 , \text{mA}$)</td>
<td>—</td>
<td>0.4 V</td>
</tr>
<tr>
<td>Output high voltage ($I_{\text{OH}} = 13 , \text{mA}$)</td>
<td>4.35 V</td>
<td>—</td>
</tr>
</tbody>
</table>

Power-on state........................................ Input (High-Z)

Data transfers ........................................ Programmed I/O

### Timing I/O

Number of channels .................................. 2 up/down counter/timers, 1 frequency scaler

Resolution
- Counter/timers ................................... 24 bits
- Frequency scaler .............................. 4 bits

Compatibility .............................. TTL/CMOS

Base clocks available
- Counter/timers .......................... 20 MHz, 100 kHz
- Frequency scaler .......................... 10 MHz, 100 kHz

Base clock accuracy ............................ ±0.01%

Max source frequency ...................... 20 MHz

Min source pulse duration ............... 10 ns, edge-detect mode

Min gate pulse duration ................. 10 ns, edge-detect mode

Data transfers ................................ DMA, interrupts, programmed I/O

DMA modes ................................. Scatter gather
Triggers

**Analog Trigger**

**Source**

- PXI-6040E and PXI-6070E..................ACH<0..15>, external trigger (PFI0/TRIG1)
- PXI-6071E........................................ACH<0..63>, external trigger (PFI0/TRIG1)

**Level** ..............................................± full-scale, internal; ±10 V, external

**Slope** ..............................................Positive or negative (software selectable)

**Resolution**........................................8 bits, 1 in 256

**Hysteresis**........................................Programmable

**Bandwidth (–3 dB)**

- PXI-6070E and PXI-6071E..................2 MHz internal, 7 MHz external
- PXI-6040E........................................650 kHz internal, 3.0 MHz external

**External input (PFI0/TRIG1)**

- **Impedance**.................................10 kΩ
- **Coupling**......................................DC
- **Protection**....................................–0.5 to \( V_{cc} + 0.5 \) V when configured as a digital signal, ±35 V when configured as an analog trigger signal or disabled, ±35 V powered off

**Digital Trigger**

**Compatibility**.................................TTL

**Response**........................................Rising or falling edge

**Pulse width**.................................10 ns min
Calibration

Recommended warm-up time .................. 15 min

Calibration interval ............................. 1 year

External calibration reference ............ >6 and <10 V

Onboard calibration reference
  Level ............................................... 5.000 V (±2.5 mV) (actual value stored in EEPROM)
  Temperature coefficient .................. ±5 ppm/° C max
  Long-term stability ......................... ±15 ppm √(t, 000 h)

Bus Interface

Type ....................................................... Master, slave

Power

Bus Requirement
  +5 VDC (±5%)
    PXI-6070E, PXI-6071E .................. 1.1 A
    PXI-6040E ............................... 0.9 A

Note  Excludes power consumed through Vcc available at the I/O connector.

I/O Connector Power
  Power available at I/O connector .......... +4.65 to +5.25 VDC at 1 A

Physical

Dimensions
  (not including connectors) ............... 16 by 10 cm (6.3 by 3.9 in)

I/O connector
  PXI-6040E, PXI-6070E .................. 68-pin male SCSI-II type
  PXI-6071E ............................... 100-pin female 0.05 D-type

Environment

Operating temperature ....................... 0° to 55° C
Storage temperature ........................................–20° to 70° C
Relative humidity ........................................5% to 90% noncondensing
Functional shock........................................MIL-T-28800 E Class 3 (per Section 4.5.5.4.1) Half-sine shock pulse, 11 ms duration, 30 g peak, 30 shocks per face
Operational random vibration..................5 to 500 Hz, 0.31 g$_{rms}$, 3 axes
Non-operational random vibration ..........5 to 500 Hz, 2.5 g$_{rms}$, 3 axes

Note Random vibration profiles were developed in accordance with MIL-T-28800E and MIL-STD-810E Method 514. Test levels exceed those recommended in MIL-STD-810E for Category 1, Basic Transportation.
PXI-6030E and PXI-6031E

Analog Input

Input Characteristics

Number of channels

- PXI-6030E ...................................... 16 single-ended or 8 differential (software-selectable)
- PXI-6031E ...................................... 64 single-ended or 8 differential (software-selectable)

Type of ADC.......................................... Successive approximation

Resolution ............................................. 16 bits, 1 in 65,536

Max sampling rate (single-channel)\(^1\) .... 100 kS/s guaranteed

Input signal ranges

<table>
<thead>
<tr>
<th>Gain (Software-Select)</th>
<th>Voltage Range (Software-Select)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Bipolar</td>
</tr>
<tr>
<td>1</td>
<td>±10 V</td>
</tr>
<tr>
<td>2</td>
<td>±5 V</td>
</tr>
<tr>
<td>5</td>
<td>±2 V</td>
</tr>
<tr>
<td>10</td>
<td>±1 V</td>
</tr>
<tr>
<td>20</td>
<td>±0.5 V</td>
</tr>
<tr>
<td>50</td>
<td>±0.2 V</td>
</tr>
<tr>
<td>100</td>
<td>±0.1 V</td>
</tr>
</tbody>
</table>

Input coupling ..................................... DC

Max working voltage ............................... Each input should remain within ±11 V of ground

\(^1\) See settling time table in Dynamic Characteristics for multichannel rates.
Appendix A Specifications for PXI-6030E and PXI-6031E

Overvoltage protection ......................±25 V powered on, ±15 V powered off

Inputs protected
PXI-6030E..............................ACH<0..15>, AISENSE
PXI-6031E..............................ACH<0..63>, AISENSE, AISENSE2

FIFO buffer size........................512 samples

Data transfers..............................DMA, interrupts, programmed I/O

DMA modes ................................Scatter gather

Configuration memory size .............512 words

Accuracy Information

See following tables
# PXI-6030E and PXI-6031E Accuracy Information

<table>
<thead>
<tr>
<th>Nominal Range (V)</th>
<th>Absolute Accuracy</th>
<th>Noise + Quantization (µV)</th>
<th>Temp Drift</th>
<th>Resolution (µV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>% of Reading</td>
<td>Offset</td>
<td>Single Pt.</td>
<td>Averaged</td>
</tr>
<tr>
<td>Positive FS</td>
<td>Negative FS</td>
<td>24 Hours</td>
<td>90 Days</td>
<td>1 Year (µV)</td>
</tr>
<tr>
<td>10</td>
<td>–10</td>
<td>0.0044%</td>
<td>0.0052%</td>
<td>0.0061%</td>
</tr>
<tr>
<td>5</td>
<td>–5</td>
<td>0.0294%</td>
<td>0.0302%</td>
<td>0.0311%</td>
</tr>
<tr>
<td>2.5</td>
<td>–2.5</td>
<td>0.0294%</td>
<td>0.0302%</td>
<td>0.0311%</td>
</tr>
<tr>
<td>1</td>
<td>–1</td>
<td>0.0294%</td>
<td>0.0302%</td>
<td>0.0311%</td>
</tr>
<tr>
<td>0.5</td>
<td>–0.5</td>
<td>0.0294%</td>
<td>0.0302%</td>
<td>0.0311%</td>
</tr>
<tr>
<td>0.25</td>
<td>–0.25</td>
<td>0.0294%</td>
<td>0.0302%</td>
<td>0.0311%</td>
</tr>
<tr>
<td>0.1</td>
<td>–0.1</td>
<td>0.0294%</td>
<td>0.0302%</td>
<td>0.0311%</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>0.0044%</td>
<td>0.0052%</td>
<td>0.0061%</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0.0294%</td>
<td>0.0302%</td>
<td>0.0311%</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0.0294%</td>
<td>0.0302%</td>
<td>0.0311%</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0.0294%</td>
<td>0.0302%</td>
<td>0.0311%</td>
</tr>
<tr>
<td>0.5</td>
<td>0</td>
<td>0.0294%</td>
<td>0.0302%</td>
<td>0.0311%</td>
</tr>
<tr>
<td>0.2</td>
<td>0</td>
<td>0.0294%</td>
<td>0.0302%</td>
<td>0.0311%</td>
</tr>
<tr>
<td>0.1</td>
<td>0</td>
<td>0.0294%</td>
<td>0.0302%</td>
<td>0.0311%</td>
</tr>
</tbody>
</table>

Absolute Accuracy = (% of Reading × Voltage) + Offset + Noise + (Temp Drift × Voltage).

Note: Temp Drift applies only if ambient is greater than ±10°C of previous external calibration.

Accuracies are valid for measurements following an internal E Series Calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings.

Measurement accuracies are listed for operational temperatures within ±1°C of internal calibration temperature and ±10°C of external or factory calibration temperature.
Transfer Characteristics

Relative accuracy.................................±0.75 LSB typ, ±1 LSB max
DNL....................................................±0.5 LSB typ, ±1 LSB max
No missing codes..............................16 bits, guaranteed

Offset error

Pregain error after calibration..........±3 µV max
Pregain error before calibration.......±2.2 mV max
Postgain error after calibration........±76 µV max
Postgain error before calibration.....±102 mV max

Gain error (relative to calibration reference)

After calibration (gain = 1).............±30.5 ppm of reading max
Before calibration.........................±2,150 ppm of reading max

With gain error adjusted to 0 at gain = 1

Gain ≠ 1 ............................................±200 ppm of reading max

Amplifier Characteristics

Input impedance

Normal, powered on ......................100 GΩ in parallel with 100 pF
Powered off .....................................820 Ω min
Overload ...........................................820 Ω min

Input bias current ..............................±1 nA
Input offset current .........................±2 nA

CMRR, DC to 60 Hz

<table>
<thead>
<tr>
<th>Gain</th>
<th>CMRR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>92 dB</td>
</tr>
<tr>
<td>2</td>
<td>97 dB</td>
</tr>
<tr>
<td>5</td>
<td>101 dB</td>
</tr>
<tr>
<td>10</td>
<td>104 dB</td>
</tr>
<tr>
<td>≥20</td>
<td>105 dB</td>
</tr>
</tbody>
</table>
Dynamic Characteristics

Bandwidth (−3 dB)
All gains .......................................... 255 kHz

Settling time for full-scale step (DC to all gains and ranges)

<table>
<thead>
<tr>
<th>Board</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>±0.00076% (±0.5 LSB)</td>
</tr>
<tr>
<td></td>
<td>±0.0015% (±1 LSB)</td>
</tr>
<tr>
<td></td>
<td>±0.0061% (±4 LSB)</td>
</tr>
<tr>
<td>PXI-6030E</td>
<td>40 µs max</td>
</tr>
<tr>
<td>PXI-6031E</td>
<td>50 µs max</td>
</tr>
</tbody>
</table>

System noise (including quantization noise)

<table>
<thead>
<tr>
<th>Gain</th>
<th>±10 V Range</th>
<th>0 to 10 V Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 to 10</td>
<td>0.6 LSB&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>0.8 LSB&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
<tr>
<td>20</td>
<td>0.7 LSB&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>1.1 LSB&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
<tr>
<td>50</td>
<td>1.1 LSB&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>2.0 LSB&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
<tr>
<td>100</td>
<td>2.0 LSB&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>3.8 LSB&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
</tbody>
</table>

Dynamic range ........................................... 91.7 dB, ±10 V input with gain 1 to 10

Crosstalk................................................. −70 dB max, DC to 100 kHz

Stability

Offset temperature coefficient

- Pregain ............................................. ±5 µV/° C
- Postgain............................................. ±120 µV/° C

Gain temperature coefficient.............. ±8 ppm/° C

Analog Output

Output Characteristics

Number of channels .................................. 2 voltage
Resolution................................................16 bits, 1 in 65,536
Max update rate ......................................100 kS/s
Type of DAC .........................................Double-buffered
FIFO buffer size.................................2,048 S
Data transfers.......................................DMA, interrupts,
programmed I/O
DMA modes .......................................Scatter gather

**PXI-6030E and PXI-6031E Accuracy Information**

<table>
<thead>
<tr>
<th>Nominal Range (V)</th>
<th>Absolute Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive FS</td>
<td>Negative FS</td>
</tr>
<tr>
<td>10</td>
<td>–10</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
</tr>
</tbody>
</table>

Absolute Accuracy = (% of Reading × Voltage) + Offset + (Temp Drift × Voltage).

**Note:** Temp drift applies only if ambient is greater than ±10° C of previous external calibration.

**Transfer Characteristics**

Relative accuracy (INL) ......................±0.5 LSB typ, ±1 LSB max

DNL..................................................±1 LSB max

Monotonicity ......................................16 bits, guaranteed
Offset error
   After calibration ............................ 305 µV max
   Before calibration ........................ 20 mV max

Gain error (relative to internal reference)
   After calibration ....................... ±30.5 ppm max
   Before calibration ................... ±2,000 ppm max

**Voltage Output**

Range ..................................................... ±10 V, 0 to 10 V
                  (software selectable)

Output coupling........................................ DC

Output impedance .................................. 0.1 Ω max

Current drive ........................................ ±5 mA

Protection .............................................. Short-circuit to ground

Power-on state ........................................ 0 V (±20 mV)

**Dynamic Characteristics**

Settling time for full-scale step .............. 10 µs to ±1 LSB accuracy

Slew rate ............................................. 5 V/µs

Noise ...................................................... 60 µVrms, DC to 1 MHz

**Stability**

Offset temperature coefficient ............ ±50 µV/° C

Gain temperature coefficient ............... ±7.5 ppm/° C

**Digital I/O**

Number of channels ......................... 8 input/output

Compatibility ........................................ TTL/CMOS
Digital logic levels

<table>
<thead>
<tr>
<th>Level</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input low voltage</td>
<td>0 V</td>
<td>0.8 V</td>
</tr>
<tr>
<td>Input high voltage</td>
<td>2 V</td>
<td>5 V</td>
</tr>
<tr>
<td>Input low current ($V_{in} = 0$ V)</td>
<td>—</td>
<td>—320 $\mu$A</td>
</tr>
<tr>
<td>Input high current ($V_{in} = 5$ V)</td>
<td>—</td>
<td>10 $\mu$A</td>
</tr>
<tr>
<td>Output low voltage ($I_{OUT} = 24$ mA)</td>
<td>—</td>
<td>0.4 V</td>
</tr>
<tr>
<td>Output high voltage ($I_{OUT} = 13$ mA)</td>
<td>4.35 V</td>
<td>—</td>
</tr>
</tbody>
</table>

Power-on state ........................................Input (High-Z)

Data transfers........................................Programmed I/O

Timing I/O

Number of channels .........................2 up/down counter/timers, 1 frequency scaler

Resolution
- Counter/timers .....................24 bits
- Frequency scaler ..................4 bits

Compatibility ..................................TTL/CMOS

Base clocks available
- Counter/timers ....................20 MHz, 100 kHz
- Frequency scaler ..................10 MHz, 100 kHz

Base clock accuracy ...................±0.01%

Max source frequency .....................20 MHz

Min source pulse duration .............10 ns, edge-detect mode

Min gate pulse duration .................10 ns, edge-detect mode

Data transfers ...................DMA, interrupts, programmed I/O

DMA modes ..................Scatter gather
Appendix A  Specifications for PXI-6030E and PXI-6031E

Triggers

Analog Trigger

Source
- PXI-6030E: ACH<0..15>, PFI0/TRIG1
- PXI-6031E: ACH<0..63>, PFI0/TRIG1

Level: ± fullscale, internal; ±10 V, external

Slope: Positive or negative (software selectable)

Resolution: 12 bits, 1 in 4,096

Hysteresis: Programmable

Bandwidth (–3 dB): 255 kHz internal, 4 MHz external

External input (PFI0/TRIG1)
- Impedance: 10 kΩ
- Coupling: DC
- Protection: 0.5 to Vcc +0.5 V when configured as a digital signal; ±35 V when configured as an analog signal or disabled; ±35 V powered off

Accuracy: ±1% of fullscale range

Digital Trigger

Compatibility: TTL

Response: Rising or falling edge

Pulse width: 10 ns min

Calibration

Recommended warm-up time: 15 min

Calibration interval: 1 year
External calibration reference ............>6 and <9.999 V

Onboard calibration reference
   Level ........................................ 5.000 V (±2.0 mV) (actual value stored in EEPROM)
   Temperature coefficient .............±0.6 ppm/° C max
   Long-term stability ......................±6 ppm/√1,000 h

Bus Interface

Type .................................................Master, slave

Power

Bus Requirements
+5 VDC (±5%) ....................................1.5 A

Note Excludes power consumed through Vcc available at the I/O connector.

I/O Connector

Power available at I/O connector.........+4.65 to +5.25 VDC at 1 A

Physical

Dimensions
   (not including connectors) ..............16 by 10 cm (6.3 by 3.9 in)

I/O connector
 PXI-6030E ........................................68-pin male SCSI-II type
 PXI-6031E ........................................100-pin female 0.05 D-type

Environment

Operating temperature ....................0 to 55° C

Storage temperature ......................−20 to 70° C

Relative humidity ............................5% to 90% noncondensing

Functional shock ............................MIL-T-28800 E Class 3 (per Section 4.5.5.4.1) Half-sine shock pulse, 11 ms duration, 30 g peak, 30 shocks per face
Operational random vibration ............... 5 to 500 Hz, 0.31 g\text{rms}, 3 axes
Non-operational random vibration ....... 5 to 500 Hz, 2.5 g\text{rms}, 3 axes

\textbf{Note}  \hspace{1em} \textit{Random vibration profiles were developed in accordance with MIL-T-28800E and MIL-STD-810E Method 514. Test levels exceed those recommended in MIL-STD-810E for Category 1, Basic Transportation.}
Optional Cable Connector Descriptions

This appendix describes the connectors on the optional cables for the PXI E Series boards.

Figure B-1 shows the pin assignments for the 68-pin E Series connector. This connector is available when you use the SH6868 or R6868 cable assemblies with the PXI-6030E, PXI-6040E, or PXI-6070E. It is also one of the two 68-pin connectors available when you use the SH1006868 cable assembly with the PXI-6031E or PXI-6071E.
### Figure B-1. 68-Pin MIO Connector Pin Assignments

<table>
<thead>
<tr>
<th>Pin</th>
<th>Pin Number</th>
<th>Pin Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACH8</td>
<td>34</td>
<td>68</td>
</tr>
<tr>
<td>ACH1</td>
<td>33</td>
<td>67</td>
</tr>
<tr>
<td>AIGND</td>
<td>32</td>
<td>66</td>
</tr>
<tr>
<td>ACH9</td>
<td>31</td>
<td>65</td>
</tr>
<tr>
<td>ACH10</td>
<td>30</td>
<td>64</td>
</tr>
<tr>
<td>AIGND</td>
<td>29</td>
<td>63</td>
</tr>
<tr>
<td>ACH11</td>
<td>28</td>
<td>62</td>
</tr>
<tr>
<td>AIGND</td>
<td>27</td>
<td>61</td>
</tr>
<tr>
<td>ACH12</td>
<td>26</td>
<td>60</td>
</tr>
<tr>
<td>ACH5</td>
<td>25</td>
<td>59</td>
</tr>
<tr>
<td>AIGND</td>
<td>24</td>
<td>58</td>
</tr>
<tr>
<td>ACH14</td>
<td>23</td>
<td>57</td>
</tr>
<tr>
<td>ACH7</td>
<td>22</td>
<td>56</td>
</tr>
<tr>
<td>AIGND</td>
<td>21</td>
<td>55</td>
</tr>
<tr>
<td>ACH15</td>
<td>20</td>
<td>54</td>
</tr>
<tr>
<td>DIO4</td>
<td>19</td>
<td>53</td>
</tr>
<tr>
<td>DGND</td>
<td>18</td>
<td>52</td>
</tr>
<tr>
<td>DIO0</td>
<td>17</td>
<td>51</td>
</tr>
<tr>
<td>DIO5</td>
<td>16</td>
<td>50</td>
</tr>
<tr>
<td>DIO2</td>
<td>15</td>
<td>49</td>
</tr>
<tr>
<td>+5 V</td>
<td>14</td>
<td>48</td>
</tr>
<tr>
<td>DIO7</td>
<td>13</td>
<td>47</td>
</tr>
<tr>
<td>DIO3</td>
<td>12</td>
<td>46</td>
</tr>
<tr>
<td>SCANCLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PFI0/TRIG1</td>
<td>11</td>
<td>45</td>
</tr>
<tr>
<td>PFI1/TRIG2</td>
<td>10</td>
<td>44</td>
</tr>
<tr>
<td>DGND</td>
<td>9</td>
<td>43</td>
</tr>
<tr>
<td>PFI2/CONVERT*</td>
<td>8</td>
<td>42</td>
</tr>
<tr>
<td>+5 V</td>
<td>8</td>
<td>41</td>
</tr>
<tr>
<td>DGND</td>
<td>7</td>
<td>40</td>
</tr>
<tr>
<td>GPCTR1_GATE</td>
<td>6</td>
<td>39</td>
</tr>
<tr>
<td>PFI5/UPDATE*</td>
<td>5</td>
<td>38</td>
</tr>
<tr>
<td>DGND</td>
<td>4</td>
<td>37</td>
</tr>
<tr>
<td>PFI7/STARTSCAN</td>
<td>3</td>
<td>36</td>
</tr>
<tr>
<td>GPCTR0_SOURCE</td>
<td>2</td>
<td>35</td>
</tr>
<tr>
<td>FREQ_OUT</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

1 Not available on the PXI-6030E and PXI-6031E
Figure B-2 shows the pin assignments for the 68-pin extended analog input connector. This is the other 68-pin connector available when you use the SH1006868 cable assembly with the PXI-6031E or PXI-6071E.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACH 24</td>
<td>34 68</td>
</tr>
<tr>
<td>ACH 17</td>
<td>33 67</td>
</tr>
<tr>
<td>ACH 18</td>
<td>32 66</td>
</tr>
<tr>
<td>ACH 27</td>
<td>31 65</td>
</tr>
<tr>
<td>ACH 20</td>
<td>30 64</td>
</tr>
<tr>
<td>ACH 21</td>
<td>29 63</td>
</tr>
<tr>
<td>ACH 30</td>
<td>28 62</td>
</tr>
<tr>
<td>ACH 23</td>
<td>27 61</td>
</tr>
<tr>
<td>ACH 32</td>
<td>26 60</td>
</tr>
<tr>
<td>ACH 41</td>
<td>25 59</td>
</tr>
<tr>
<td>ACH 34</td>
<td>24 58</td>
</tr>
<tr>
<td>ACH 35</td>
<td>23 57</td>
</tr>
<tr>
<td>AIGND</td>
<td>22 56</td>
</tr>
<tr>
<td>ACH 44</td>
<td>21 55</td>
</tr>
<tr>
<td>ACH 37</td>
<td>20 54</td>
</tr>
<tr>
<td>ACH 38</td>
<td>19 53</td>
</tr>
<tr>
<td>ACH 47</td>
<td>18 52</td>
</tr>
<tr>
<td>ACH 48</td>
<td>17 51</td>
</tr>
<tr>
<td>ACH 49</td>
<td>16 50</td>
</tr>
<tr>
<td>ACH 58</td>
<td>15 49</td>
</tr>
<tr>
<td>ACH 51</td>
<td>14 48</td>
</tr>
<tr>
<td>ACH 52</td>
<td>13 47</td>
</tr>
<tr>
<td>ACH 61</td>
<td>12 46</td>
</tr>
<tr>
<td>ACH 54</td>
<td>11 45</td>
</tr>
<tr>
<td>ACH 55</td>
<td>10 44</td>
</tr>
<tr>
<td>N/C</td>
<td>9 43</td>
</tr>
<tr>
<td>N/C</td>
<td>8 42</td>
</tr>
<tr>
<td>N/C</td>
<td>7 41</td>
</tr>
<tr>
<td>N/C</td>
<td>6 40</td>
</tr>
<tr>
<td>N/C</td>
<td>5 39</td>
</tr>
<tr>
<td>N/C</td>
<td>4 38</td>
</tr>
<tr>
<td>N/C</td>
<td>3 37</td>
</tr>
<tr>
<td>N/C</td>
<td>2 36</td>
</tr>
<tr>
<td>N/C</td>
<td>1 35</td>
</tr>
</tbody>
</table>

*Figure B-2. 68-Pin Extended Analog Input Connector Pin Assignments*
Figure B-3 shows the pin assignments for the 50-pin MIO connector. This connector is available when you use the SH6850 or R6850 cable assemblies with the PXI-6030E, PXI-6040E, or PXI-6070E. It is also one of the two 50-pin connectors available when you use the R1005050 cable assembly with the PXI-6031E or PXI-6071E.

![Figure B-3. 50-Pin MIO Connector Pin Assignments](image-url)
Common Questions

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of your PXI E Series board.

General Information

What are the PXI E Series boards?
The PXI E Series boards are switchless and jumperless enhanced MIO boards that use the DAQ-STC for timing.

What is the DAQ-STC?
The DAQ-STC is the system timing control application-specific integrated circuit (ASIC) designed by National Instruments and is the backbone of the PXI E Series boards. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into three groups:

- Analog input—two 24-bit, two 16-bit counters
- Analog output—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be configured independently with timing resolutions of 50 ns or 10 μs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities such as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate are possible.

What type of 5 V protection do the PXI E Series boards have?
The PXI E Series boards have 5 V lines equipped with a self-resetting 1 A fuse.
### Installation and Configuration

**How do you set the base address for a PXI E Series board?**

The base address of a PXI E Series board is assigned automatically through the PXI bus protocol. This assignment is completely transparent to you.

**What jumpers should I be aware of when configuring my PXI E Series board?**

The PXI E Series boards are jumperless and switchless.

**Which National Instruments document should I read first to get started using DAQ software?**

Your NI-DAQ or application software release notes documentation is always the best starting place.

**What version of NI-DAQ must I have to program my PXI E Series board?**

You must have the NI-DAQ for PC compatibles version 5.1 or higher.

### Analog Input and Output

**I’m using my board in differential analog input mode and I have connected a differential input signal, but my readings are random and drift rapidly. What’s wrong?**

Check your ground reference connections. Your signal may be referenced to a level that is considered floating with reference to the board ground reference. Even if you are in differential mode, the signal must still be referenced to the same ground level as the board reference. There are various methods of achieving this while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in Chapter 4, *Signal Connections*.

**I’m using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?**

When it switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. You can build a lowpass deglitching filter to remove some of these glitches, depending on the
frequency and nature of your output signal. The PXI-6070E and PXI-6071E boards have built-in reglitchers, which can be software-enabled, on its analog output channels. See the Analog Output Reglitch Selection section in Chapter 3, Hardware Overview, for more information about reglitching.

**Can I synchronize a one-channel analog input data acquisition with a one-channel analog output waveform generation on my PXI E Series board?**

Yes. One way to accomplish this is to use the waveform generation timing pulses to control the analog input data acquisition. To do this, follow steps 1 through 4 below, in addition to the usual steps for data acquisition and waveform generation configuration.

1. Enable the PFI5 line for output, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW).
   - If you are using LabVIEW, invoke Route Signal VI with signal name set to PFI5 and signal source set to AO Update.

2. Set up data acquisition timing so that the timing signal for A/D conversion comes from PFI5, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_IN_CONVERT, ND_PFI_5, ND_HIGH_TO_LOW).
   - If you are using LabVIEW, invoke AI Clock Config VI with clock source code set to PFI pin, high to low, and clock source string set to 5.

3. Initiate analog input data acquisition, which will start only when the analog output waveform generation starts.
4. Initiate analog output waveform generation.

**Timing and Digital I/O**

**What types of triggering can be hardware-implemented on my PXI E Series board?**

Digital triggering is hardware-supported on every PXI E Series board. In addition, the PXI-6030E, PXI-6031E, PXI-6040E, PXI-6070E and PXI-6071E support analog triggering in hardware.
What added functionality does the DAQ-STC make possible in contrast to the Am9513?

The DAQ-STC incorporates much more than just 10 Am9513-style counters within one chip. In fact, the DAQ-STC has the complexity of more than 24 chips. The DAQ-STC makes possible PFI lines, analog triggering, selectable logic level, and frequency shift keying. The DAQ-STC also makes buffered operations possible, such as direct up/down control, single or pulse train generation, equivalent time sampling, buffered period, and buffered semiperiod measurement.

What is the difference in timebases between the Am9513 counter/timer and the DAQ-STC?

The DAQ-STC-based MIO boards have a 20 MHz timebase. The Am9513-based MIO boards have a 1 MHz or 5 MHz timebase.

Will the counter/timer applications that I wrote Am9513 work with the DAQ-STC?

If you are using NI-DAQ with LabVIEW, some of your applications written using the CTR VIs will still run. However, there are many differences in the counters between the PXI E Series and other boards; the counter numbers are different, timebase selections are different, and the DAQ-STC counters are 24-bit counters (unlike the 16-bit counters on boards without the DAQ-STC).

If you are using the NI-DAQ language interface or LabWindows/CVI, the answer is no, the counter/timer applications that you wrote previously will not work with the DAQ-STC. You must use the GPCTR functions; ICTR and CTR functions will not work with the DAQ-STC. The GPCTR functions have the same capabilities as the ICTR and CTR functions, plus more, but you must rewrite the application with the GPCTR function calls.

I’m using one of the general-purpose counter/timers on my PXI E Series board, but I do not see the counter/timer output on the I/O connector. What am I doing wrong?

If you are using the NI-DAQ language interface or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the Select_Signal call in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are tri-stated.
What are the PFIs and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

If you are using the NI-DAQ language interface or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, CTR Mode Config, and CTR Pulse Config advanced level VIs to indicate which function the connected signal will serve. Use the Route Signal VI to enable the PFI lines to output internal signals.

¡Caution! If you enable a PFI line for output, do not connect any external signal source to it; if you do, you can damage the board, the computer, and the connected equipment.

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high impedance by the hardware. This means that the board circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in Table 4-1. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) will be in the high impedance state after power on, and Table 4-1 shows that there is a 50 kΩ pull-up resistor. This pull-up resistor will set the DIO(0) pin to a logic high when the output is in a high impedance state.
Customer Communication

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve your technical problems and a form you can use to comment on the product documentation. When you contact us, we need the information on the Technical Support Form and the configuration form, if your manual contains one, about your system configuration to answer your questions as quickly as possible.

National Instruments has technical assistance through electronic, fax, and telephone systems to quickly provide the information you need. Our electronic services include a bulletin board service, an FTP site, a fax-on-demand system, and e-mail support. If you have a hardware or software problem, first try the electronic support systems. If the information available on these systems does not answer your questions, we offer fax and telephone support through our technical support centers, which are staffed by applications engineers.

Electronic Services

Bulletin Board Support
National Instruments has BBS and FTP sites dedicated for 24-hour support with a collection of files and documents to answer most common customer questions. From these sites, you can also download the latest instrument drivers, updates, and example programs. For recorded instructions on how to use the bulletin board and FTP services and for BBS automated information, call 512 795 6990. You can access these services at:

- United States: 512 794 5422
  - Up to 14,400 baud, 8 data bits, 1 stop bit, no parity
- United Kingdom: 01635 551422
  - Up to 9,600 baud, 8 data bits, 1 stop bit, no parity
- France: 01 48 65 15 59
  - Up to 9,600 baud, 8 data bits, 1 stop bit, no parity

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<thead>
<tr>
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<th>Fax</th>
</tr>
</thead>
<tbody>
<tr>
<td>Australia</td>
<td>03 9879 5166</td>
<td>03 9879 6277</td>
</tr>
<tr>
<td>Austria</td>
<td>0662 45 79 90 0</td>
<td>0662 45 79 90 19</td>
</tr>
<tr>
<td>Belgium</td>
<td>02 757 00 20</td>
<td>02 757 03 11</td>
</tr>
<tr>
<td>Brazil</td>
<td>011 288 3336</td>
<td>011 288 8528</td>
</tr>
<tr>
<td>Canada (Ontario)</td>
<td>905 785 0085</td>
<td>905 785 0086</td>
</tr>
<tr>
<td>Canada (Quebec)</td>
<td>514 694 8521</td>
<td>514 694 4399</td>
</tr>
<tr>
<td>Denmark</td>
<td>45 76 26 00</td>
<td>45 76 26 02</td>
</tr>
<tr>
<td>Finland</td>
<td>09 725 725 11</td>
<td>09 725 725 55</td>
</tr>
<tr>
<td>France</td>
<td>01 48 14 24 24</td>
<td>01 48 14 24 14</td>
</tr>
<tr>
<td>Germany</td>
<td>089 741 31 30</td>
<td>089 714 60 35</td>
</tr>
<tr>
<td>Hong Kong</td>
<td>2645 3186</td>
<td>2686 8505</td>
</tr>
<tr>
<td>Israel</td>
<td>03 6120092</td>
<td>03 6120095</td>
</tr>
<tr>
<td>Italy</td>
<td>02 413091</td>
<td>02 41309215</td>
</tr>
<tr>
<td>Japan</td>
<td>03 5472 2970</td>
<td>03 5472 2977</td>
</tr>
<tr>
<td>Korea</td>
<td>02 596 7456</td>
<td>02 596 7455</td>
</tr>
<tr>
<td>Mexico</td>
<td>5 520 2635</td>
<td>5 520 3282</td>
</tr>
<tr>
<td>Netherlands</td>
<td>0348 433466</td>
<td>0348 430673</td>
</tr>
<tr>
<td>Norway</td>
<td>32 84 84 00</td>
<td>32 84 86 00</td>
</tr>
<tr>
<td>Singapore</td>
<td>2265886</td>
<td>2265887</td>
</tr>
<tr>
<td>Spain</td>
<td>91 640 0085</td>
<td>91 640 0533</td>
</tr>
<tr>
<td>Sweden</td>
<td>08 730 49 70</td>
<td>08 730 43 70</td>
</tr>
<tr>
<td>Switzerland</td>
<td>056 200 51 51</td>
<td>056 200 51 55</td>
</tr>
<tr>
<td>Taiwan</td>
<td>02 377 1200</td>
<td>02 737 4644</td>
</tr>
<tr>
<td>United Kingdom</td>
<td>01635 523545</td>
<td>01635 523154</td>
</tr>
<tr>
<td>United States</td>
<td>512 795 8248</td>
<td>512 794 5678</td>
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Computer brand____________ Model ___________________ Processor _____________________
Operating system (include version number) __________________________________________
Clock speed ______MHz   RAM _____MB   Display adapter __________________________
Mouse ___yes ___no     Other adapters installed _______________________________________
Hard disk capacity _____MB   Brand_________________________________________________
Instruments used ________________________________________________________________
_______________________________________________________________________________
National Instruments hardware product model _____________ Revision ____________________
Configuration ___________________________________________________________________
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Interrupt level of PXI E Series board _________________________________________________
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Software version _________________________________________________________________

Other Products

Computer make and model _________________________________________________________
Microprocessor __________________________________________________________________
Clock frequency or speed _________________________________________________________
Type of video board installed _____________________________________________________
Operating system version _________________________________________________________
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Edition Date: January 1999
Part Number: 321554C-01

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# Glossary

## Prefix Meanings

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<th>Meanings</th>
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<tr>
<td>p-</td>
<td>pico</td>
<td>$10^{-12}$</td>
</tr>
<tr>
<td>n-</td>
<td>nano-</td>
<td>$10^{-9}$</td>
</tr>
<tr>
<td>µ-</td>
<td>micro-</td>
<td>$10^{-6}$</td>
</tr>
<tr>
<td>m-</td>
<td>milli-</td>
<td>$10^{-3}$</td>
</tr>
<tr>
<td>k-</td>
<td>kilo-</td>
<td>$10^3$</td>
</tr>
<tr>
<td>M-</td>
<td>mega-</td>
<td>$10^6$</td>
</tr>
<tr>
<td>G-</td>
<td>giga-</td>
<td>$10^9$</td>
</tr>
</tbody>
</table>

## Numbers/Symbols

- ° degrees
- > greater than
- ≥ greater than or equal to
- < less than
- ≤ less than or equal to
- – negative of, or minus
- Ω ohms
- / per
- % percent
- ± plus or minus
- + positive of, or plus
A

A

amperes

AC

alternating current

ACH

analog input channel signal

A/D

analog-to-digital

ADC

analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number

AI

analog input

AIGATE

analog input gate signal

AIGND

analog input ground signal

AISENSE

analog input sense signal

ANSI

American National Standards Institute

AO

analog output

AOGND

analog output ground signal

ASIC

Application-Specific Integrated Circuit—a proprietary semiconductor component designed and manufactured to perform a set of specific functions.

B

BIOS

basic input/output system—BIOS functions are the fundamental level of any PC or compatible computer. BIOS functions embody the basic operations needed for successful use of the computer’s hardware resources.

bipolar

a signal range that includes both positive and negative values (for example, −5 V to +5 V)
C

Celsius

CalDAC calibration DAC

CH channel—pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.

centimeter

CMOS complementary metal-oxide semiconductor

CMRR common-mode rejection ratio—a measure of an instrument’s ability to reject interference from a common-mode signal, usually expressed in decibels (dB)

CompactPCI Refers to the core specification defined by the PCI Industrial Computer Manufacturer’s Group (PICMG)

Convert convert signal

counter/timer a circuit that counts external pulses or clock pulses (timing)

counter

D

digital-to-analog

digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current

analog channel 0 output signal

analog channel 1 output signal

data acquisition—a system that uses the computer to collect, receive, and generate electrical signals
Glossary

DAQ-STC  A custom ASIC implementing a system timing controller for data-acquisition time-related functions. The DAQ-STC consists of three timing groups that control analog input, analog output, and general-purpose counter/timer functions.

dB  decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB=20log10 V1/V2, for signals in volts

DC  direct current

DGND  digital ground signal

DIFF  differential mode

DIO  digital input/output

DIP  dual inline package

dithering  the addition of Gaussian noise to an analog input signal

DMA  direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.

DNL  differential nonlinearity—a measure in LSB of the worst-case deviation of code widths from their ideal value of 1 LSB

DO  digital output

E  EEPROM  electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed

EXTREF  external reference signal

EXTSTROBE  external strobe signal
FIFO first-in first-out memory buffer—FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be read or written. For example, an analog input FIFO stores the results of A/D conversions until the data can be read into system memory. Programming the DMA controller and servicing interrupts can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored in the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.

FREQ_OUT frequency output signal

ft feet

GATE gate signal

GPCTR general purpose counter

GPCTR0_GATE general purpose counter 0 gate signal

GPCTR1_GATE general purpose counter 1 gate signal

GPCTR0_OUT general purpose counter 0 output signal

GPCTR1_OUT general purpose counter 1 output signal

GPCTR0_SOURCE general purpose counter 0 clock source signal

GPCTR1_SOURCE general purpose counter 1 clock source signal

GPCTR0_UP_DOWN general purpose counter 0 up down

GPCTR1_UP_DOWN general purpose counter 1 up down

$g_{\text{rms}}$ level of random vibration
Glossary

H

h    hour
hex  hexadecimal
Hz   hertz

I

I/O  input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
I_{OH}  current, output high
I_{OL}  current, output low
INL   relative accuracy

L

LSB  least significant bit

M

m    meter
MB   megabytes of memory
MIO  multifunction I/O
MITE MXI Interfaces to Everything is a custom ASIC designed by National Instruments that implements the PCI bus interface. The MITE supports bus mastering for high speed data transfers over the PCI bus.
MSB  most significant bit
mux  multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel
### Glossary

**N**

- **NC** normally closed, or not connected
- **NI-DAQ** NI driver software for DAQ hardware
- **noise** an undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
- **NRSE** nonreferenced single-ended mode—all measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground

**O**

- **OUT** output pin—a counter output pin where the counter can generate various TTL pulse waveforms

**P**

- **PCI** Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 MB/s.
- **pd** pulldown
- **PFI** Programmable Function Input
- **PFI0/TRIG1** PFI0/trigger 1
- **PFI1/TRIG2** PFI1/trigger 2
- **PFI2/CONVERT** PFI2/convert
- **PFI3/GPCTR1_** PFI3/general purpose counter 1 source
- **SOURCE**
- **PFI4/GPCTR1_GATE** PFI4/general purpose counter 1 gate
**Glossary**

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<th>Definition</th>
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<td>PFI5/update</td>
</tr>
<tr>
<td>PFI6/WFTRIG</td>
<td>PFI6/waveform trigger</td>
</tr>
<tr>
<td>PFI7/STARTSCAN</td>
<td>PFI7/start of scan</td>
</tr>
<tr>
<td>PFI8/GPCTR0_SOURCE</td>
<td>PFI8/general purpose counter 0 source</td>
</tr>
<tr>
<td>PFI9/GPCTR0_GATE</td>
<td>PFI9/general purpose counter 0 gate</td>
</tr>
<tr>
<td>PGIA</td>
<td>Programmable Gain Instrumentation Amplifier</td>
</tr>
<tr>
<td>port</td>
<td>(1) a communications connection on a computer or a remote controller (2) a digital port, consisting of four or eight lines of digital input and/or output</td>
</tr>
<tr>
<td>ppm</td>
<td>parts per million</td>
</tr>
<tr>
<td>pu</td>
<td>pull-up</td>
</tr>
<tr>
<td>PXI</td>
<td>Stands for PCI eXtensions for Instrumentation. PXI is an open specification that builds off the CompactPCI specification by adding instrumentation-specific features.</td>
</tr>
<tr>
<td>RAM</td>
<td>random access memory</td>
</tr>
<tr>
<td>rms</td>
<td>root mean square</td>
</tr>
<tr>
<td>RSE</td>
<td>referenced single-ended mode—all measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system.</td>
</tr>
<tr>
<td>RTD</td>
<td>resistive temperature detector—a metallic probe that measures temperature based upon its coefficient of resistivity</td>
</tr>
<tr>
<td>RTSIbus</td>
<td>Real-time system integration bus—the National Instruments timing bus that connects DAQ boards directly for precise synchronization of functions. This connection is made across the PXI trigger bus.</td>
</tr>
</tbody>
</table>
S

s seconds

S samples

SCANCLK scan clock signal

SCXI Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ boards in the noisy computer environment

SE single-ended—a term used to describe an analog input that is measured with respect to a common ground

settling time the amount of time required for a voltage to reach its final value within specified limits

signal conditioning the manipulation of signals to prepare them for digitizing

SISOURCE SI counter clock signal

SOURCE source signal

S/s samples per second—used to express the rate at which a DAQ board samples an analog signal

STARTSCAN start scan signal

system noise a measure of the amount of noise seen by an analog circuit or an ADC when the analog inputs are grounded

T

TC terminal count—the ending value of a counter

t_{gh} gate hold time

t_{gsu} gate setup time

t_{gw} gate pulse width

t_{out} output delay time
### Glossary

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</tr>
</thead>
<tbody>
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<td>THD</td>
<td>total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in dB or percent</td>
</tr>
<tr>
<td>thermocouple</td>
<td>a temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of the temperature.</td>
</tr>
<tr>
<td>TRIG</td>
<td>trigger signal</td>
</tr>
<tr>
<td>tsc</td>
<td>source clock period</td>
</tr>
<tr>
<td>tsp</td>
<td>source pulse width</td>
</tr>
<tr>
<td>TTL</td>
<td>transistor-transistor logic</td>
</tr>
<tr>
<td>UI</td>
<td>update interval</td>
</tr>
<tr>
<td>UISOURCE</td>
<td>update interval counter clock signal</td>
</tr>
<tr>
<td>unipolar</td>
<td>a signal range that is always positive (for example, 0 to +10 V)</td>
</tr>
<tr>
<td>UPDATE</td>
<td>update signal</td>
</tr>
<tr>
<td>V</td>
<td>volts</td>
</tr>
<tr>
<td>VDC</td>
<td>volts direct current</td>
</tr>
<tr>
<td>VI</td>
<td>virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program</td>
</tr>
<tr>
<td>V_{IH}</td>
<td>volts, input high</td>
</tr>
<tr>
<td>V_{IL}</td>
<td>volts, input low</td>
</tr>
<tr>
<td>V_{in}</td>
<td>volts in</td>
</tr>
<tr>
<td>V_{m}</td>
<td>measured voltage</td>
</tr>
<tr>
<td>V_{OH}</td>
<td>volts, output high</td>
</tr>
<tr>
<td><strong>V</strong></td>
<td><strong>volts, output low</strong></td>
</tr>
<tr>
<td>------------</td>
<td>----------------------</td>
</tr>
<tr>
<td><strong>V^\text{ref}</strong></td>
<td><strong>reference voltage</strong></td>
</tr>
<tr>
<td><strong>V^\text{rms}</strong></td>
<td><strong>volts, root mean square</strong></td>
</tr>
</tbody>
</table>

**W**

<table>
<thead>
<tr>
<th><strong>waveform</strong></th>
<th><strong>multiple voltage readings taken at a specific sampling rate</strong></th>
</tr>
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<td><strong>WFTRIG</strong></td>
<td><strong>waveform generation trigger signal</strong></td>
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