Reconfigurable Chassis for NI CompactRIO

NI cRIO-911x NEW!

- Easy-to-use LabVIEW FPGA automatically synthesizes electrical circuit implementation
- RIO FPGA core executes at default rates of 40 MHz, and can be compiled to run even faster
- Design hardware in LabVIEW
- 4- or 8-slot chassis for any CompactRIO I/O module
- DIN-rail mount, 19 in. rack mount, and panel mount options
- NI CompactRIO Extreme Industrial Certifications and Ratings

Overview and Applications
NI CompactRIO reconfigurable chassis are the heart of the CompactRIO system because they contain the reconfigurable I/O (RIO) core. You program the RIO field-programmable gate array (FPGA) core, which has an individual connection to each I/O module, with easy-to-use elemental I/O functions to read or write signal information from each module. Because there is no shared communication bus between the RIO FPGA core and the I/O modules, you can precisely synchronize I/O operations on each module with 25 ns resolution. The RIO core can perform local integer-based or fixed-point signal processing and decision making and directly pass signals from one module to another. It is connected to the CompactRIO real-time controller through a local PCI bus interface. The real-time controller can retrieve data from any control or indicator on the RIO FPGA application front panel through an easy-to-use scan interface or simple FPGA Read/Write function. The RIO FPGA can also generate interrupt requests (IRQs) to synchronize the real-time software execution with the RIO FPGA. Typically, the real-time controller is used to convert the integer-based I/O data to scaled floating-point numbers. In addition, it performs single-point control, waveform analysis, data logging, and Ethernet/serial communication. The reconfigurable chassis, real-time controller, and I/O modules combine to create a complete stand-alone embedded system.

Key Features
- Create any local or timing, triggering, and synchronization scheme with 25 ns resolution
- Use multiple while loops to create a parallel processing application for high-performance signal processing or multirate control systems
- Take advantage of built-in proportional integral derivative (PID) control functions for control system loop rates greater than 100 kHz
- Generate waveforms or implement nonlinear lookup tables (LUTs) using LabVIEW FPGA Express VIs
- Integrate widely available third-party HDL cores using the LabVIEW FPGA Module HDL Node
- Enforce critical logic and interlocks in silicon hardware circuitry, or use the parallel RIO architecture to create dual, triple, or quadruple redundant systems

Visit ni.com/compactrio for example programs, application notes, and other developer tools.

<table>
<thead>
<tr>
<th>Model</th>
<th>Module Slots</th>
<th>FPGA</th>
<th>LUTs and Flip-Flops</th>
<th>FPGA Multipliers</th>
<th>FPGA Block RAM (kb)</th>
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<td>Virtex-5 LX30</td>
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Table 1. Chassis Comparison Table
Reconfigurable Chassis for NI CompactRIO

New Virtex-5 FPGAs
New NI cRIO-911x chassis use Virtex-5 FPGAs with improved optimization capabilities to help you execute code faster and increase code capacity. These FPGAs feature a new six-input LUT architecture for substantially improved resource utilization as well as DSP48 slices that make it possible for you to implement more complex digital signal processing at faster rates. Previous-generation Virtex-II FPGAs use four-input LUTs for up to 16 combinations of digital logic values. The new Virtex-5 FPGAs use six-input LUTs for up to 64 combinations, increasing the amount of logic that you can implement per slice. In addition, the slices themselves are placed in closer proximity to each other to reduce the propagation delay of electrons and increase overall execution rates. The single-cycle timed loop structure in LabVIEW FPGA takes full advantage of six-input LUTs for substantially improved resource utilization. This means you can optimize more LabVIEW FPGA code to fit within Virtex-5 FPGAs and perform more operations per clock cycle.

![Figure 1. General logic benchmarks show that Virtex-5 FPGAs offer larger sizes than Virtex-II FPGAs.](image1)

![Figure 2. Execution speed benchmarks show that Virtex-5 FPGAs feature faster processing capabilities than Virtex-II FPGAs.](image2)

Ordering Information

| NI cRIO-9111 | 780915-01 |
| NI cRIO-9112 | 780916-01 |
| NI cRIO-9113 | 780917-01 |
| NI cRIO-9114 | 780918-01 |
| NI cRIO-9116 | 780919-01 |

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System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

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