Southern Africa Large Telescope

Prime Focus Imaging Spectrograph

SAAO Detector Subsystem:

SALT-3196AE0001: Detector Document

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Issue History

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SALT-3196AE0001 Detector Issue 2.1.doc	EFB	2.1	28 Nov 2002	Added Sub-System Controller Section
SALT-3196AE0001 Detector Issue 2.2.doc	EFB	2.2	01 Dec 2002	Fixed some errors in Sub-systems Controller Section
SALT-3196AE0001 Detector Issue 2.3.doc	DBC	2.3	05 Dec 2002	First major edit for CDR
SALT-3196AE0001 Detector Issue 2.4.doc	DBC	2.4	11 Feb 2003	Inserting mosaicing information.
SALT-3196AE0001 Detector Issue 2.5.doc	DBC	2.5	20 Feb 2003	Insert SDSU controller performance and final touch-ups for CDR.
SALT-3196AE0001 Detector Issue 2.6.doc	DBC	2.6	11 Mar 2003	Add 3rd PFIS CCD parameters and fix some formatting problems

Table of Contents

1 Scope

This document reports a design study for the Detector Subsystem of the University of Wisconsin-Madison's Prime Focus Imaging Spectrograph (PFIS). It specifies the performance that the Detector Subsystem could meet to satisfy the overall performance goals of the spectrograph.

CCD procurement was recognized to be a long lead time purchase and a contract was concluded with Marconi Applied Technologies in January 2002 to secure devices for the two SALT first light instruments. (Note: in July 2002, Marconi Applied Technologies became E2V but for the remainder of this document, they will still be referred to as Marconi)

2 Overview

The detector subsystem will comprise a cryostat containing a 3x1 mini-mosaic of CCD chips. These chips shall be Marconi 44-82 CCDs with 2k x 4k x 15 micron pixels. They shall be mounted on an invar cold plate and it is decided that SAAO will do the mosaicing in order to achieve co-planarity of the devices. The mosaic shall be housed in an evacuated cryostat and thermally connected to the cold end of a Cryotiger, which shall cool the chips sufficiently to render dark current insignificant, whilst at the same time reducing QE by the smallest extent possible. The detectors shall be managed by an SDSU III CCD controller, which will in turn be controlled by a PC.

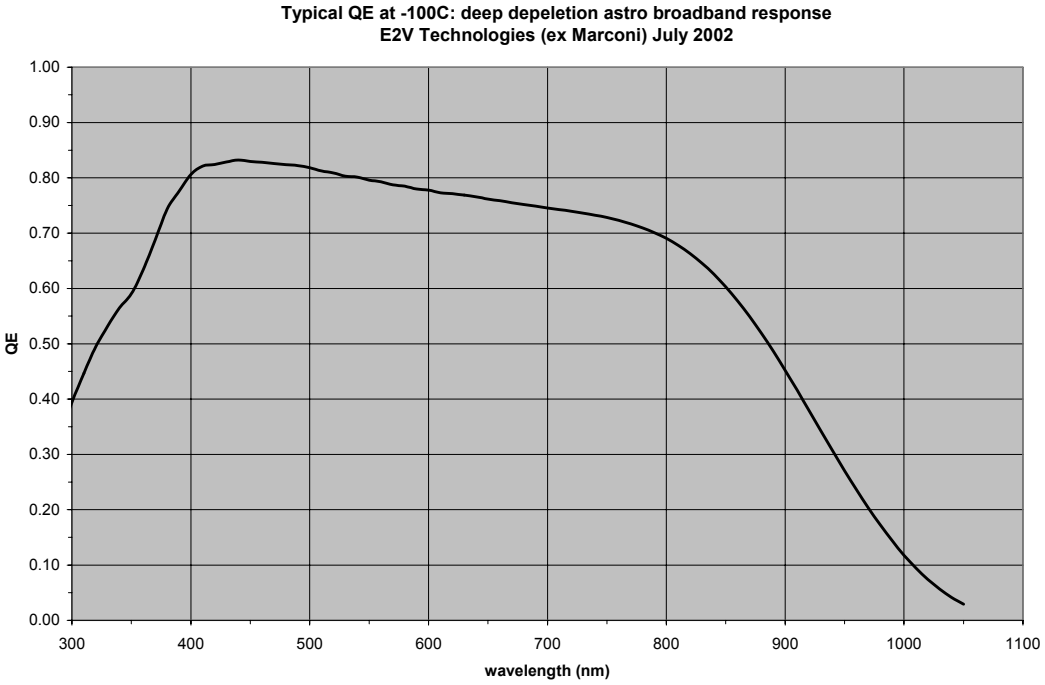
3 The CCDs

In terms of a contract between the SALT Foundation and Marconi, the latter will supply their CCD 44-82 chips for use as the PFIS detectors. Other potential sources of chips were discussed in the PDR version of this document, saao.design-study.doc, which should be consulted for details.

3.1 Basic Parameters

The CCD characteristics may be obtained from the Marconi data sheets, the most important details of which are reproduced below. In this list, guaranteed (min or max as appropriate) as well as (more generous) typical figures are quoted:

- 2048 x 4096 x 15 micron square pixels
- 30.7 x 61.4 mm^2 imaging area
- Thinned and back-illuminated
- 3-side buttable
- 2 output amplifiers
- Charge transfer efficiency: min: 99.999 per cent, typical 99.9995 per cent
- Pixel readout frequency 20-1000 kHz
- Peak signal (full well): min: 150 k e^-/pix, typical: 200 k e^-/pix
- Readout noise (at 188 K, 20 kHz): max: 4.0 e^-/pix, typical: 2.5 e^-/pix
- QE at 500 nm: 80 per cent
- Spectral range: 200-1060 nm
- Dark current (at 153 K): max: 4, typical: 0.1 e^-/pix/hr.



3.2 Sensitivity

Dr. Paul Jorden of Marconi has provided the above plot (Fig. 1) showing typical performance for Marconi deep depletion silicon and Astro BB anti-reflection coating devices, which have been selected for PFIS.

However, it must be remembered that the plot shows "typical" performance figures (i.e. the mean of a large sample of Marconi devices). Any specific device may not achieve this performance. Marconi have undertaken to guarantee minimum performance as specified in the table below, shown alongside the "typical" sensitivity for comparison:

Table 1 Table 1 CCD Spectral Response

Wave-length	Minimum QE	Typical QE	**SALT-03**	**SALT-04**	**SALT-05**
350 nm	>40%	50%	**79.9**	**66.5**	**50.6**
400 nm	>70%	80%	**86.0**	**79.2**	**71.7**
500 nm	>75%	80%	**85.0**	**79.6**	**77.7**
650 nm	>70%	75%	**75.5**	**74.4**	**70.1**
900 nm	>45%	50%	**45.4**	**46.8**	**45.1**
1000 nm	No spec	No spec	**10.8**	**10.7**	**10.0**

At the time of writing, three science grade devices have been delivered; and their properties are shown in Table 1 under the columns SALT-03, SALT-04 and SALT-05.

3.3 Frame Transfer Architecture

In order to enable rapid spectroscopy, FT operation is essential. None of the large format devices made by Marconi are available off the shelf in Frame Transfer (FT) Mode. Marconi are supplying FT chips in terms of the contract with SALT. This requires a redesign of the clock lines of the chip and therefore a special production run from Marconi. The completion date for the order for the PFIS devices is end February 2003.

3.4 Mini-Mosaic

A mini-mosaic of 3x1 CCDs will be used. Mosaicing will be carried out by SAAO. See Section 8.

3.5 Cosmetics

In terms of the contract between SALT and Marconi, the latter may supply grade 0 (preferably) or grade 1 (minimum) devices. The numerical definition of these specifications is shown in Table 2, along with the acceptance test reports for the first two devices.

Table 2 CCD Grade Blemish Specification

Defects	Grade 0	Grade 1	**SALT-03**	**SALT-04**	**SALT-05**
Column defects (black or white)	6 or less	12 or less	**2**	**0**	**0**
White spots	500 or less	1000 or less	**122**	**107**	**21**
Total spots (black or white)	1250 or less	2000 or less	**128**	**116**	**33**
Traps	30 or less	50 or less	**0**	**0**	**7**

3.6 Dark Current and Operating Temperature

The performance goal for dark current is to ensure that noise on the dark current pedestal generated during the longest exposure is small compared to the readout noise. We estimate that, with minimum readout noise of 2.5 e^-/pix, a dark current rate of 1 e^-/pix/longest exposure will fulfill this satisfactorily. The longest exposure is expected to be about 1 hr. So dark current rate of no more than 1 e^-/pix/hr is proposed. From the typical dark current rate on the Marconi data sheet (0.1 e^-/pix/hr at 153 K) and the $T^3 e^{-6400/T}$ scaling with temperature specified by Marconi, this implies an operating temperature of 163 K or less. Measured dark currents in the first three devices are 0.71, 0.014 and 0.023 e^-/pix.

3.7 Readout Noise

Marconi guarantee a readout noise from the on-chip amplifier of 4.0 e^-/pix at a readout speed of 20 kHz. 2.5 e^-/pix is typical. A plot in the data sheet shows this typical figure rising to 5.5 e^-/pix at the maximum certified speed of 1000 kHz. It might be expected that the maximum readout noise from the on-chip amplifier at 1000 kHz would be 4.0/2.5 x 5.5 = 8.8 e^-/pix. We expect the SDSU II controller and additional electronics to add 1.5 e^-/pix (assuming a gain of 1 e^-/ADU). We thus propose the following readout noise performance:

- 3.0 e^-/pix at 100 kHz (10.0 μsec/pix)
- 5.0 e^-/pix at 380 kHz (3 μsec/pix)

These values are **TBC1**.

In terms of the Marconi contract, at a readout speed of 20000 pixels/sec, the readout noise must be less than 4 electrons per pixel RMS for all science grade SALT CCDs with typical performance of 2.5 electrons per pixel RMS. The first three PFIS chips have the following performance:

	SALT-03	SALT-04	SALT-05
Readout Noise (e^-/pix)	**2.3 & 2.2**	**2.0 & 2.4**	**1.9 & 1.9**

Note: Two values for each device are listed because each device has a split output serial register (readout register) and two output amplifiers.

4 CCD Controller

Images are obtained by clearing all charge from the CCD detectors, exposing them to light and reading them out with the CCD controller which will be an SDSU III (Leach) controller from Astronomical Research Cameras (San Diego). CCD readout proceeds by clocking the charge in each pixel towards the readout amplifier where it is measured, digitised and sent to the control computer. A schematic of the chip architecture is shown in Fig. 2 (not drawn to scale).

The Marconi CCDs have a split readout register with a readout amplifier at either end; each readout amplifier is preceded by 50 extra pixels which are never exposed to light.

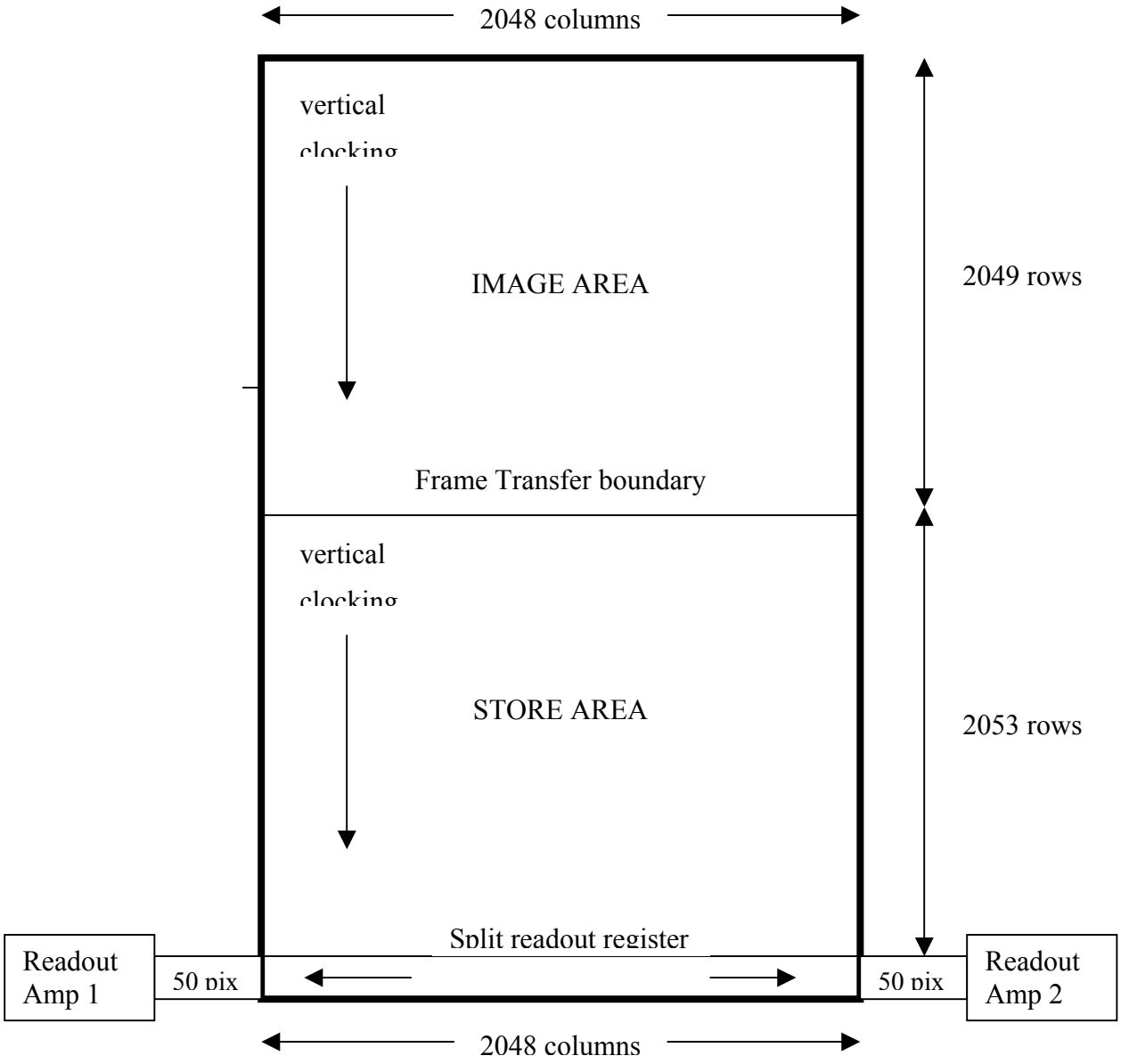


Figure 2. CCD architecture for Marconi 44-82 devices

The readout noise associated with the charge measurement process results in a compromise between readout speed and noise: the faster the readout the higher the readout noise. Readout speed is increased if the pixels are combined before being fed through the readout amplifier which is where most time is required. Pixel combination, or prebinning, effectively combines 2 or more rows into the readout register, or 2 or more pixels into one with the combined charge before being fed into the readout amplifier. Windowing is also a possible means of speeding up readout in which pixels in the

readout register which lie outside the desired window are “skipped” rapidly.

Frame transfer operation is another way to reduce readout time further. When operated this way, half of each chip closest to the readout register is masked from light (labeled “Store Area” in Fig. 2; see also Fig. 3). At the end of an exposure, a frame transfer takes place (in 0.10 sec) transferring the image formed in the half of the chip furthest from the readout register (labeled “Image Area” in Fig. 2) to behind the mask. Readout of the masked region proceeds as the next exposure is accumulating. In addition to reducing the amount of data to be read out, this technique has the advantage that there is no “dead time” during read out. The shutter is open throughout this sequence. The field of view is, of course, halved with frame transfer operation.

The controller will have 4 video channels allowing the use of the two available output amplifiers per CCD chip.

4.1 Readout Speed

Marconi certify performance in the range 20-1000 kHz. The SDSU III controller allows readout rates of no more than 1000 kPix/s.

Due to the need for real Marconi chips with which to conduct tests, we will use performance estimates from Guy Woodhouse, a CCD engineer we know well who worked on La Palma and now works on the fast CCD camera for the Faint Object Spectrograph for Subaru. Guy has solid experience with the same kind of Marconi chips and SDSU controllers. For the present, we thus aim to match the performance he reports. (However, recent communication from Vikram Dhillon of Sheffield University (U.K.), reporting on the Ultracam instrument commissioning run, indicates that a degree of caution should be exercised when predicting readout speeds with Marconi detectors. The Ultracam experience was that the vertical clock times achieved with good performance were significantly longer than those predicted by Marconi. The Ultracam detectors are AIMO devices, and PFIS uses non-AIMO detectors, thus the relevance of this report to PFIS is uncertain.)

Correlated Double Sampling (CDS) speeds of 3.0 μsec/pix (at 5 e^-/pix readout noise) or 4.6 μsec/pix (at 3.5 e^-/pix readout noise) have been achieved with the proposed chips and SDSU controllers by Guy. It may be possible to reduce the 3.0 μsec/pix (with readout noise penalty) but this remains to be investigated. This figure increases linearly with horizontal prebin factor by approximately 1.0μsec/pix. Windowing also adds some overhead to the total readout time (TBC**2**).

We therefore propose a discrete set of normal pixel readout rates in the range 100-333 kHz (**TBC3**) and software selectable (slower readout rates would result in unacceptably long readout times). In addition, drift scan and charge shuffling during exposure will

require special control of the vertical clocks which will be synchronized at a software selectable rate.

Overheads are also associated with row transfers, 50 μsec per row, and pixel skips in the readout register (discards) of 1.0 μsec/pix (**TBC4**).

Each CCD has 4102 rows, 2048 columns and 2 readout amplifiers. There are an additional 50 pixels at the end of each readout register but before the readout amplifier. Thus, readout requires feeding 4106 rows of (1024+50) columns, or a total of 4405548 pixels, through each readout amplifier.

The following sections discuss various readout modes such as prebin, window, frame transfer and slot mode, and show example calculations of readout time for various combinations. Section 5 gives a more detailed analysis of readout time.

4.2 Lowest Noise Full Frame Readout

Lowest readout noise is expected at the slowest readout rate of 100 kHz (10 μsec/pix). Readout times at this rate would be:

- **Time to clear the chip prior to exposure or time for vertical transfers during readout: 4102*50 μsec = 0.2051 sec**
- **Time to read out the full chip (without prebinning):**
  0.2051 sec + 4405548*10.0 μsec = 44.196 sec (readout noise of 3 e^-/pix: TBC1)

4.3 Rapid Full Frame Readout

The above timing considerations give rise to the following expected performance when high time resolution is desired:

- **Minimum time to read out the full chip (without prebinning):**
  0.2051 sec + 4405548*3.0 μsec = 13.422 sec (readout noise of 5 e^-/pix)

Readout time can be decreased further by any one of (or combinations thereof):

- Frame transfer operation so that only half the detector is used. There is no readout dead time as the next exposure is accumulating during the readout.
- Prebinning (see next section)
- Windowing of the chip either in the spatial or wavelength direction or both

4.4 Prebinning

Software-selectable prebinning of 1x1 to 9x9 (independent in each dimension) will be offered. It is expected that at least 1x2 prebinning will be used as standard where the 2 refers to the spatial direction. For all but the highest resolution observations, 2x2 prebinning will be used. Such prebinning will then result in minimum readout times of:

- **1x2 prebinning: 0.2051 sec + 2202774*11.0 μsec = 24.435 sec (3 e^-/pix readout noise: TBC1)**
- **2x2 prebinning: 0.2051 sec + 1101387*11.0 μsec = 12.320 sec (3 e^-/pix readout noise: TBC1)**
- **1x2 prebinning: 0.2051 sec + 2202774*4.0 μsec = 9.016 sec (5 e^-/pix readout noise)**
- **2x2 prebinning: 0.2051 sec + 1101387*4.0 μsec = 4.611 sec (5 e^-/pix readout noise)**

We believe there will be a 1 μsec overhead for each horizontal prebinning increment (essentially the time to combine pixels during readout). However, this is **TBC5**.

4.5 Frame Transfer Operation

Frame Transfer capability will be provided by the CCD controller. In this mode, at the end of an exposure of the half of the chip furthest from the readout register (the image section of the chip), the data are rapidly shifted (in 0.102 sec) into the half of the chip next to the readout register (the store section). (illustrated in Fig. 2)Readout of the store section then takes place. Naturally, the store section of the chip must be masked from light so that half the science FoV must be sacrificed. The shutter is open throughout the sequence of operations.

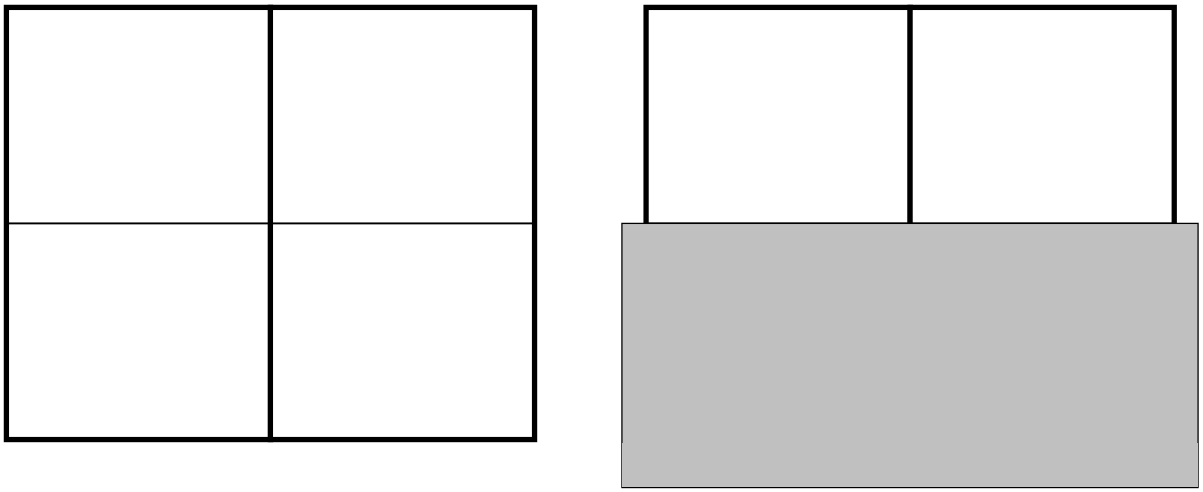


Figure 3. Full frame operation is depicted in the left schematic. The right schematic shows frame transfer operation with the frame transfer mask obscuring half of the detector

Minimum readout times are (with 4102 vertical transfers required because although only 2053 are required to move the image into the store area, vertical transfers in the store area are still required):

- **No prebinning: 102*50 μsec + (1074*205348*10.0) μsec = 22.254 sec (3 e^-/pix readout noise)**
- **1x2 prebinning: 4102*50 μsec + (1074*1027*11.0) μsec = 12.338 sec (3 e^-/pix readout noise).**
- **2x2 prebinning: 4102*50 μsec + (537*1027*11.0) μsec = 6.271 sec (3 e^-/pix readout noise).**
- **No prebinning: 4102*50 μsec + (1074*2053*3.0) μsec = 6.82 sec (5 e^-/pix readout noise)**
- **1x2 prebinning: 4102*50 μsec + (1074*1027*4.0) μsec = 4.617 sec (5 e^-/pix readout noise).**
- **2x2 prebinning: 4102*50 μsec + (537*1027*4.0) μsec = 2.411 sec (5 e^-/pix readout noise).**

Thus, a continuous sequence of images with 2.41.8 sec sampling and no dead time can be obtained. Image smearing will occur during the 0.102 sec needed for frame transfer.

4.6 Windowing

Readout of up to 10 windows (**TBC6**) of rectangular shape and arbitrary size will be offered by the CCD controller. Note that a window defined on one half of one CCD chip

is also applied to the other half, as well as replicated twice on each of the other two chips. This is because the readout through each amplifier must use the same clocking scheme. The implication of this for spectroscopy is that windowing in the dispersion direction will result in 6 discrete wavelength intervals being readout. The scientific value of windowing in the dispersion direction in spectroscopy seems limited (but perhaps not zero).

Two examples will illustrate the readout rate possible with windowed operation. The performance in these examples must certainly be confirmed (**TBC7**).

In the first, a spectrum is to be obtained of a point source located near the middle of the chip, just above the frame transfer boundary, with wavelength range spanning the full width of the detector in dispersion, and 8.64 arcsec (64 pixels) in the cross dispersion direction. Assuming frame transfer operation and 2x2 prebinning, the minimum readout time would be:

$$0.205 \text{ sec} + (32*537*4.0)\ \mu\text{sec} = 0.273 \text{ sec}$$

Where the first contribution (0.205 sec) is the time taken to shift the spectrum down by roughly half a frame (to the readout register) and the time needed for vertical transfers in the store section of the chip. The second contribution (0.068 sec) is the time taken to read out the 32 x 537 pixels. However, the image would be exposed for only 0.050 sec and there would be 0.205 sec of dead time, so unacceptable smearing would result.

The 0.205 sec contribution could be eliminated, thereby yielding spectroscopy at a speed of faster than 10 Hz, if the spectrum is shifted just over the frame transfer boundary, rather than all the way down to the readout register. The minimum readout time would then be:

(64*50) μsec + (64*50) μsec + (32*537*4.0) μsec

= 0.0032 sec + 0.0032 sec + 0.068 sec

= 0.0744 sec

A sequence of such spectra could then be obtained with a cycle time of **0.090 sec** (allowing 0.016 seconds for safety) and image smearing over a 0.0032 sec interval.

The second example is an imaging example in which a target and two comparison stars are to be sampled rapidly by reading out three 128x128 boxes of pixels centred on the three objects. In full frame mode (i.e. shuttered), but 2x2 prebinning, the minimum readout time would involve:

- 0.205 sec for vertical transfers,
- (3*64*(1074-128)*1.0) μsec for pixel skipping and
- (3*64*64*4.0) μsec for pixel reads. These contributions are:

0.2051 sec + 0.181 sec + 0.049 sec = 0.435 sec

once again dominated by the time for vertical transfers. Frame transfer operation would cut this time in half.

4.7 Gain

The SDSU controller allows the gain to be scaled by one of four preset factors: x1; x2; x4.75; x9.5. The base gain can be set by adjusting the electronics and this is still to be decided: **TBD1**.

5 Readout Speed Analysis

As high time resolution is a niche scientific area, and in response to a request following the PDR, this section seeks to clarify the issue of readout time. We present formulae for calculating readout speeds for the various readout modes. The following definitions apply:

Rows	4102. An array of 4102 columns. There are 4102 rows (4096+6) that are simultaneously clocked down the device towards the readout register.
Cols	1074. An array of 2148 pixels (2048+50+50) that is clocked serially to the output amplifier. The array is split in two and has two outputs operating in parallel, thus the effective size of the array is 1074 pixels.
P_{dat}	Data Pixel. A pixel that forms part of the required image data. It can be binned or unbinned, part of a window or full frame/frame transfer image.
P_{skip}	Skip Pixel. A pixel in the Columns array that is not part of the required image data. Skip pixels have to be clocked out of the detector, thus degrade performance by "wasting" readout time.
PB_{col}	The columns prebin factor. Range of 1 to 9
PB_{row}	The rows prebin factor. Range of 1 to 9
T_{row}	50μS. Time required to do one row shift. Marconi specifies 100μS, but various communications indicate that 50μS is a realistic time for fast clocking of small signal levels.
T_{col}	1.0μS. Time required to shift the serial register by one pixel.
T_{proc}	2.0μS (fast) & 9.0μS (slow). Overhead time associated with signal processing on each data pixel.

5.1 Readout speed calculations

We now give some examples, repeating the calculations of Section 4 and adding some new cases. Note that windowed readout almost requires a different formula for each case!

Example 1. Full Frame Readout, slow, unbinned:

$T = (rows * T_{row}) + (cols * rows * (T_{col} + T_{proc}))$

$= (4102 * 50) + (1074 * 4102 * (1.0 + 9.0))$ μS

= 44.3 seconds

Example 2. Full Frame Readout, fast, unbinned:

$T = (rows * T_{row}) + (cols * rows * (T_{col} + T_{proc}))$

$= (4102 * 50) + (1074 * 4102 * (1.0 + 2.0))$ μS

= 13.4 seconds

Example 3. Frame Transfer Readout, fast, unbinned:

$T = (rows * T_{row}) + (cols * (rows/2) * (T_{col} + T_{proc}))$

$= (4102 * 50) + (1074 * 4102/2 * (1.0 + 2.0))$ μS

= 6.81 seconds

In normal use, PFIS will be read out in prebinned mode. For this case, the above formula becomes:

$T = (rows * T_{row}) + ((cols/PB_{col}) * (rows/PB_{row}) * ((T_{col} * PB_{col}) + T_{proc}))$

Example 4. Full Frame readout, fast, binned 2*2:

$T = (4102 * 50) + ((1074/2) * (4102/2) * ((1.0 * 2) + 2.0))$ μS

= 4.61 seconds

Example 5. Frame Transfer readout, fast, binned 2*2:

$T = (4102 * 50) + ((1074/2) * (4102/(2*2)) * ((1.0 * 2) + 2.0))$ μS

= 2.41 seconds

Example 6. Full Frame readout, fast, binned 4*4:

$T = (4102 * 50) + ((1074/4) * (4102/4) * ((1.0 * 4) + 2.0))$ μS

= 1.86 seconds

Example 7. Frame Transfer readout, fast, binned 4*4:

$T = (4102 * 50) + ((1074/4) * (4102/(4*2)) * ((1.0 * 4) + 2.0))$ μS

= 1.03 seconds

Note that binning does not gain a factor of PB_{col}* PB_{row} as might naively be expected. It certainly gains a factor of PB_{row}, but the gain in binning in the output register is offset by the fact that the relevant pixels have to be shifted anyway.

PFIS also allows windowed (sub-array) readout. The window may be binned or unbinned. Window mode readout can be done in both full frame and frame transfer mode. As multiple windows are allowed, the readout time calculation becomes increasingly complex.

Example 8. One window (actually two due to the parallel operation of the two outputs of the CCD), binned 2x2:

For this case, more variables have to be defined:

WC 100. Number of unbinned columns in window

PWC 99. Number of unbinned columns to discard before the start of the window

WR 100. Number of unbinned rows in window

PWR 100. Number of unbinned columns to discard before the start of the window

N 875. Number of unbinned columns to discard after the window such that

N = Cols – (WC + PWC)

The formula becomes:

$$T = (Rows * T_{row}) + [(WC/PB_{col}) * (WR/PB_{row}) * ((T_{col} * PB_{col}) + T_{proc})] + [WR/ PB_{row} * ((PWC + N) * T_{col})]$$

This formula can be expressed as: (Total row transfer time) + (total binned window time) + (total unbinned pre-and-post window time)

$$T = (4102 * 50) + [(100/2) * (100/2) * ((1.0 * 2) + 2.0)] + [100/2 * ((99 + 875) * 1.0)]$$

= 0.26 seconds

Table 3: PFIS Readout times

PFIS Readout times (in seconds)						
Readout Mode	**lowest noise** 2x2 binning	**Highest speed, various binning factors** 1x1	2x2	3x3	4x4	9x9
Full Frame	12.3	13.4	4.6	2.7	1.9	0.80
Frame Transfer	6.3	6.8	2.4	1.4	1.0	0.50
Full Frame, 1 window (100x100)	0.28	0.33	0.26	0.24	0.23	0.22
Full Frame, 2 windows same row (100x100)	0.30	0.35	0.27	0.24	0.23	0.22
Full Frame, 2 windows separate rows (100x100)	0.36	0.46	0.32	0.28	0.26	0.23

Additional values are shown in Table 3. They were calculated using a Readout time calculator set up in the file

Readout time calcs.xls

This is available to any interested party.

In all cases in Table 3 of full frame readout or frame transfer readout , the "smearing time" or row transfer time, is 0.205 sec. This is apparent as a tendency for the readout times to converge on this number as the prebinning gets larger and larger.

6 SDSU Controller Configuration

6.1 Introduction

An important design decision to be made regarding the SDSU controller configuration for PFIS is the number of clock boards necessary to drive the 3-device mini-mosaic. This affects the size of the controller crate, which has size & mass implications for the instrument.

The standard SDSU controller configuration is a 6-slot card frame. For PFIS, the following minimum number of PCBs are required:

Timing Board x1

Utility board x1

Clock board x1

Video Board x3 (The PFIS detector package has three CCDs each with two outputs, each SDSU video board has two channels)

Thus for the PFIS detector system the 6-slot card frame will be fully populated.

If more than one clock board is required to drive the PFIS mosaic, the SDSU 12-slot card frame will have to be used. This is a much larger and heavier box than the 6-slot card frame.

There has been some doubt as to whether the SDSU clock board can successfully drive multiple CCD detectors. Opinions sought from users of the SDSU controller have ranged from "I have done this and it was fine" to "I wouldn't want to try to do that". Many groups use the SDSU controller with E2V 2Kx4K detectors apparently satisfactorily.

As part of the preparatory work for the PFIS detector system, SAAO has performed tests using the SALTICAM detector hardware to evaluate the ability of the SDSU clock board to drive multiple CCDs. Provisional results are presented here.

6.2 Tests Performed

Due to a number of delays to the SALTICAM project it has not been possible to do actual performance tests (i.e. Charge Transfer Efficiency and image smearing) at this time. The tests done involved evaluating the SDSU clock board driver capabilities by examining the image area clock waveforms when driving different configurations and numbers of CCDs with a single SDSU clock driver board. The test results in the form of oscilloscope screenshots are presented below.

6.3 CCD Image area Clock structure – a primer

CCDs have a system of clock electrodes laid across the imaging area which are used to define pixel positions and to move signal charge towards the output node. The E2V devices as used in SALT detector packages have three clock phases per pixel. During exposure time unvarying voltages are applied to these phases in a low-high-low pattern, and signal charge accumulates under the "high" clock. To read out the CCD the clock phases alternate between a high and low voltage in a fixed pattern to move the signal charge along. I refer to this fixed clock pattern as a "triplet" in this document. One clock triplet moves the signal charge along by one pixel. Figure 6.1 is an example of such a clock triplet. The triplet is repeated 4102 times in the case of the CCD44-82 detector to move the entire image down to the readout register.

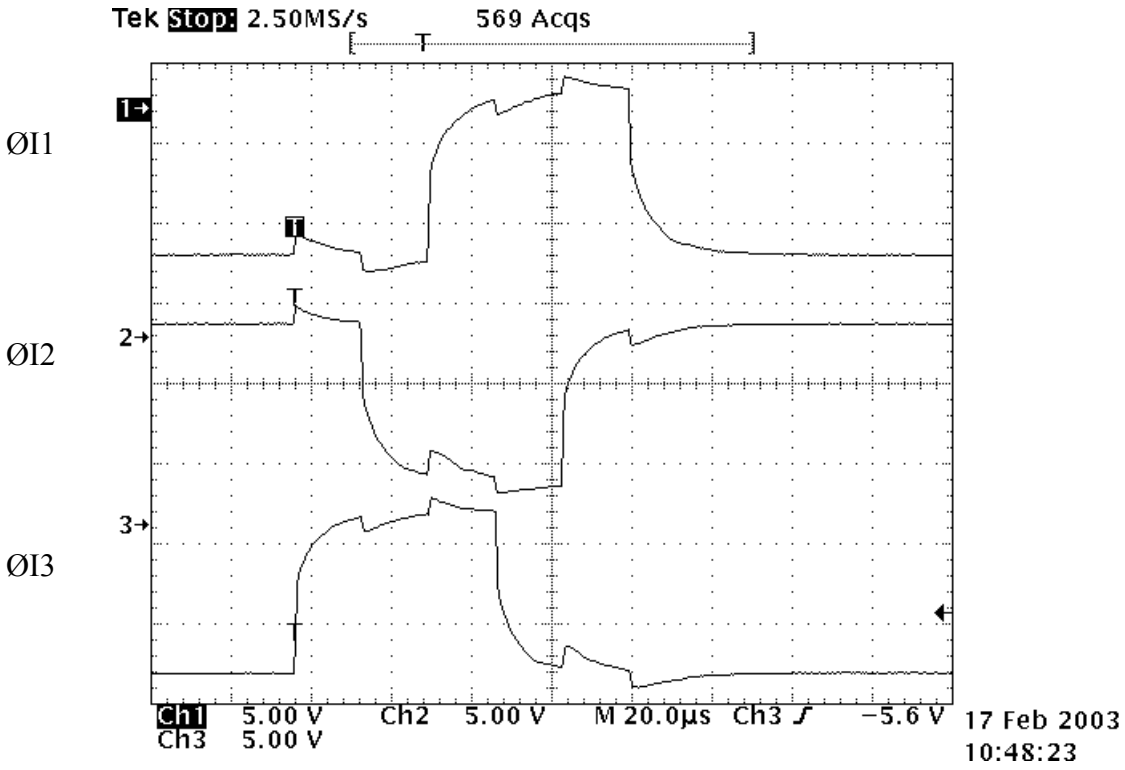


Figure 6.1: CCD Image Area Clock Triplet

From Figure 6.1 note:

1. Clock pulse width 50µs
2. Clock overlap T_o is ~16µs
3. Rise time T_r of ØI1 is ~16µs, fall time T_f is ~14 µs
4. Clock Triplet time ~110µs including fall time of last clock edge.

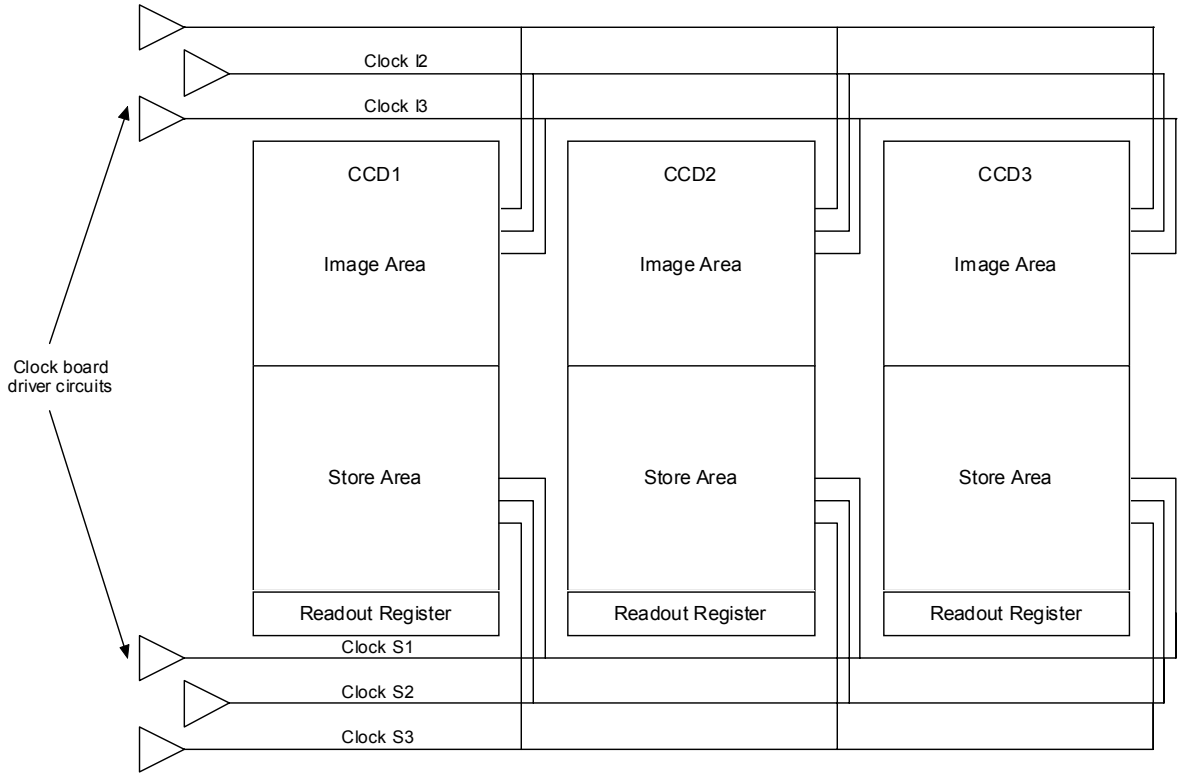


Figure 6.2: PFIS detectors clock connection scheme

Due to their close proximity to each other in the CCD structure, the clock electrodes form capacitors with each other and with the substrate of the CCD. The crosstalk evident between clock phases in Figure 6.1 is an artifact of this capacitive coupling.

The above discussion serves to introduce the fact that the CCD image area clock electrodes present a relatively high capacitive load to the controller electronics clock driver circuits. This concept is crucial for a correct evaluation of the test results below. Capacitive loads introduce clock rise/fall time limits on the maximum speed (minimum clock pulse width) achievable with a given clock driver circuit.

CCDs are available in full-frame and frame-transfer architecture. In the full-frame CCD, the image area clock electrodes are brought out to three pins on the device connector. A frame-transfer CCD has the image area divided into two halves designated image and store areas, the three image area clocks are brought out to three pins and the three store area clocks are brought out to an additional three pins on the device connector. The SALT CCD44-82 detectors are frame transfer CCDs.

For the purposes of these tests I have defined each CCD as representing two equal clock loads – image area clocks and store area clocks. A non-frame-transfer CCD has image & store area clocks connected together on-chip, and thus counts as two loads. A frame transfer CCD has image and store area clocks wired independently to pins on the device

connector. Three frame-transfer CCDs as used in the PFIS detector system total 6 loads. Figure 6.2 shows a clock connection scheme for the PFIS detector package using one clock board.

6.4 Test Results

Tests were done using an oscilloscope to examine the clock waveforms with different load combinations and clock pulse widths.

6.4.1 Waveforms with clock pulse width=50µs, Row transfer time=100µs

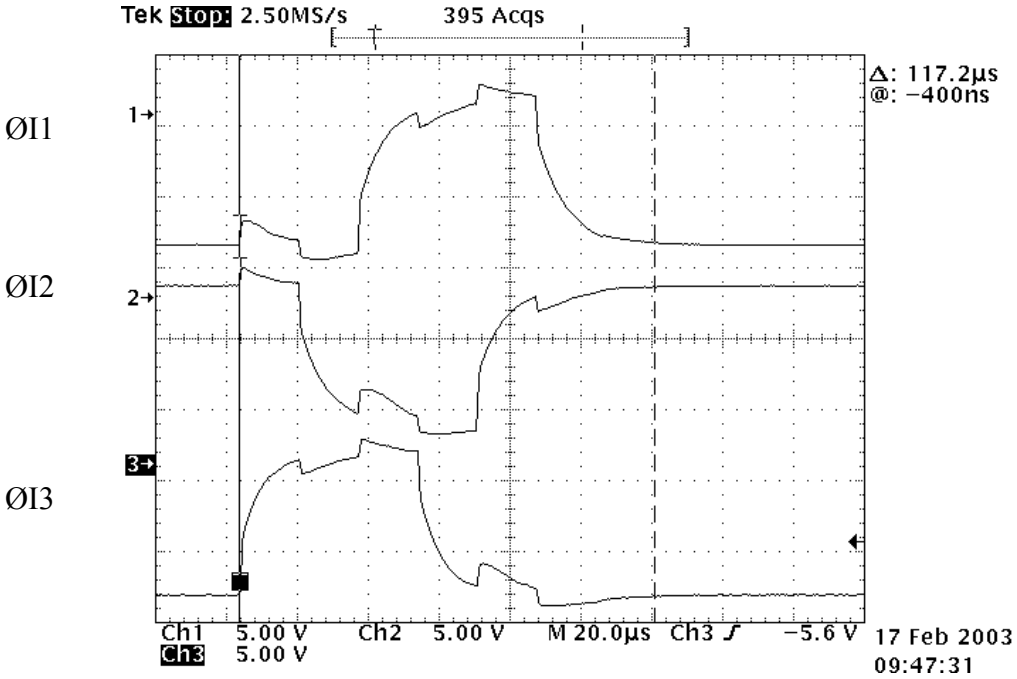


Figure 6.3: Image area clock triplet, three loads

Figure 6.3 shows the waveforms we expect to see with the PFIS detector system when using one clock board, where each clock driver circuit has three loads as defined in section 3. The datasheet "typical" clock pulse width of 50µs is used.

This looks acceptable, but in fact contravenes some of the specifications for image area clock rise time (T_r) and clock overlap (T_o) as defined in the CCD44-82 data sheet. The results are discussed in detail in section 4.3 and section 5.

Figures 4 through 7 show expanded views of one clock waveform for each case of one load through four loads, with rise/fall time measurements.

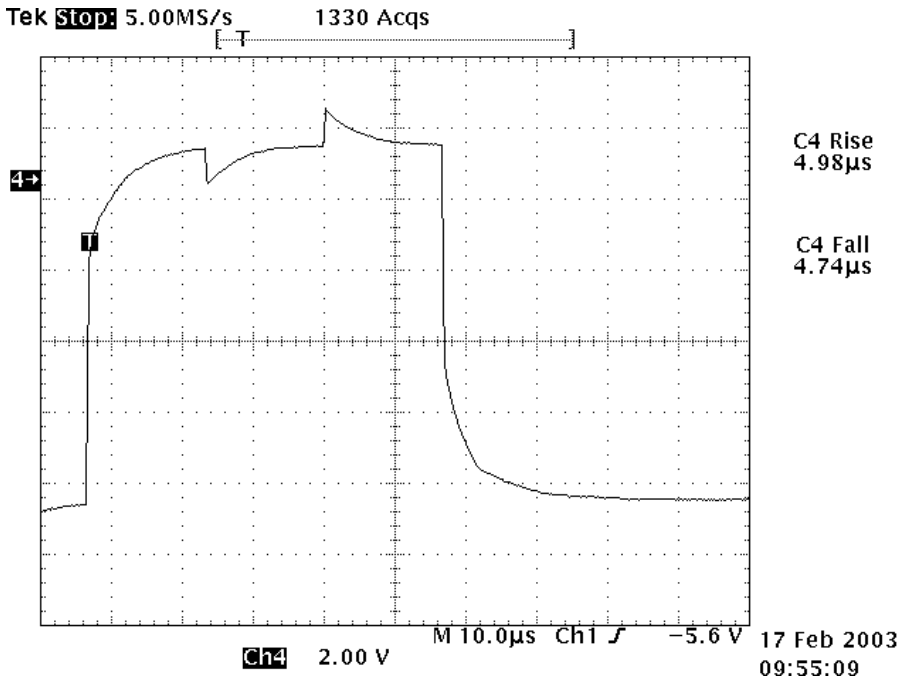


Figure 6.4: One load (store area of one frame-transfer CCD)

T_r: 5µs; T_o: 14µs: this is within the E2V specifications

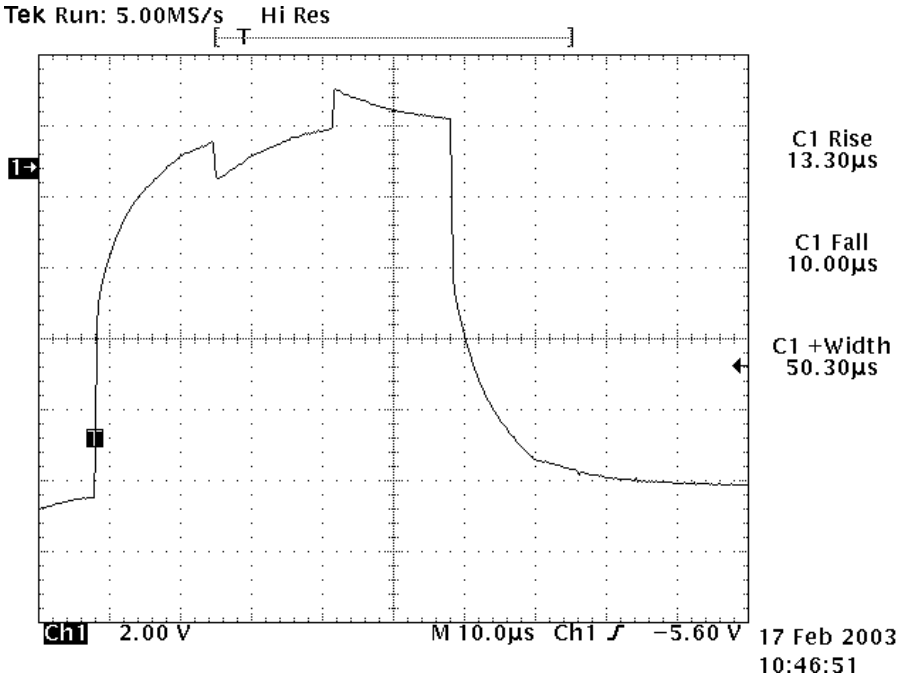


Figure 6.5: Two Loads (one frame transfer CCD)

T_r: 13µs; T_o: 14µs: this does not comply with the E2V specification of $T_r < 0.5\ T_o$.

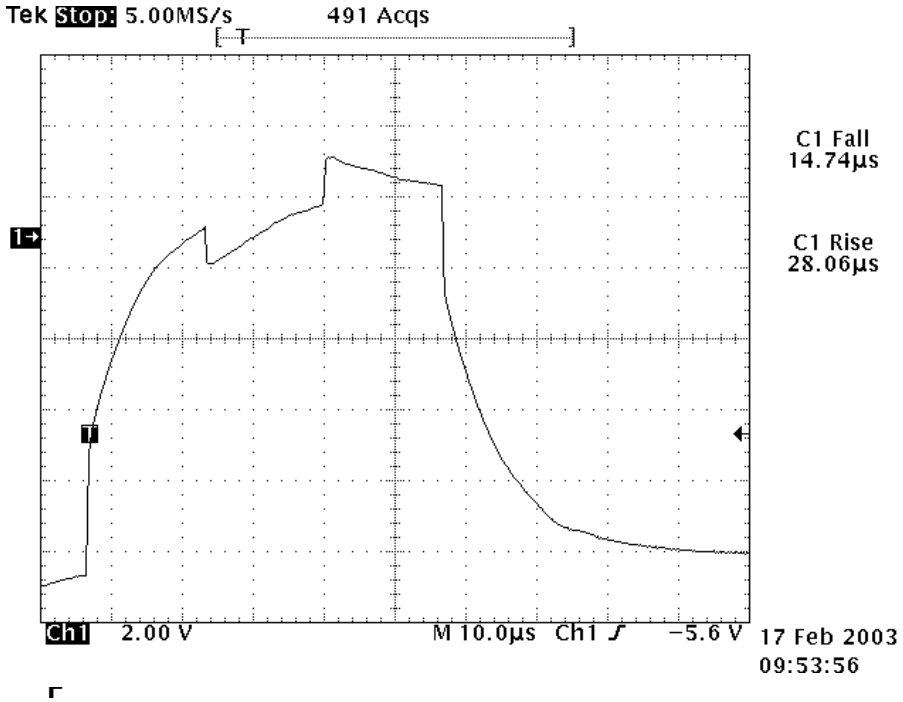


Figure 6.6: Three loads (as for PFIS detector package)

T_r: 28µs; T_o: 14µs: this does not comply with the E2V specification of $T_r < 0.5\ T_o$.

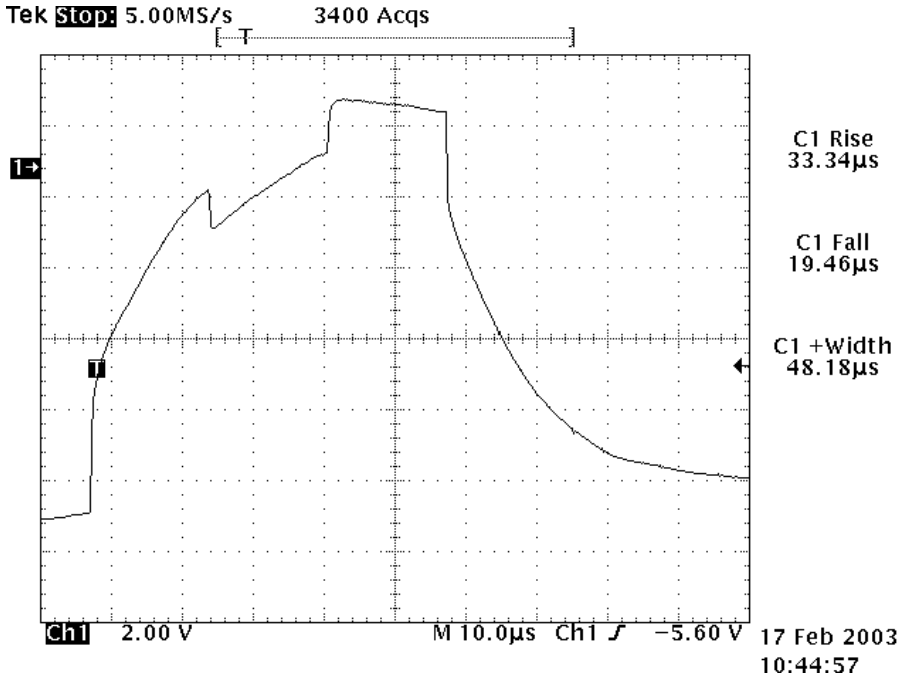


Figure 6.7: Four loads (two frame transfer CCDs)

T_r: 33µs; T_o: 14µs: this does not comply with the E2V specification of $T_r < 0.5\ T_o$.

6.4.2 Waveforms with clock pulse width=25µs, Row transfer time=50µs

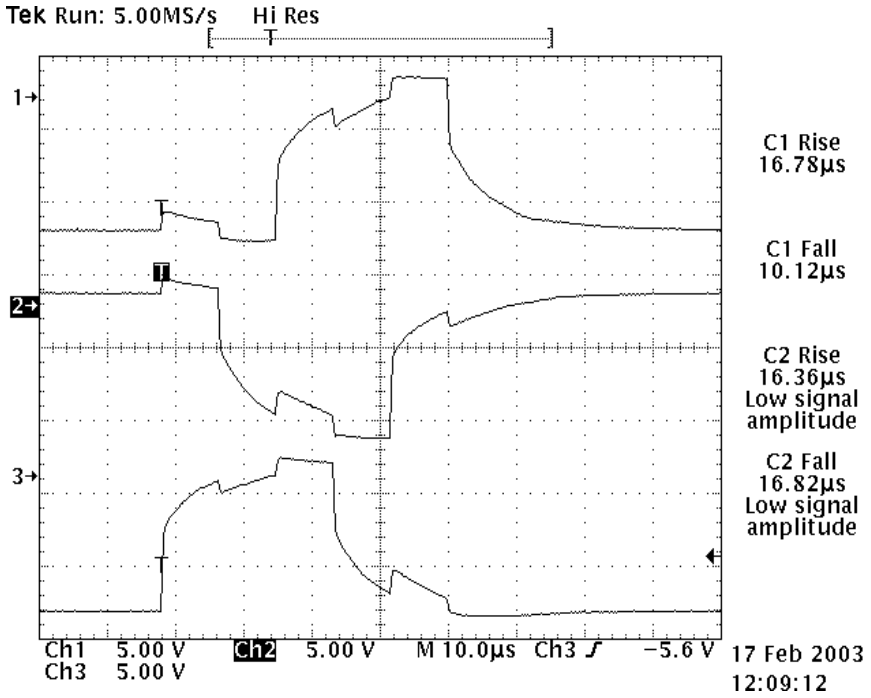


Figure 6.8: image area clock triplet, two loads

Notes: 1. Clock pulse width 25µs.
2. Clock Triplet time ~55µs including fall time of last clock edge.
3. Clock overlap is ~8.3µs

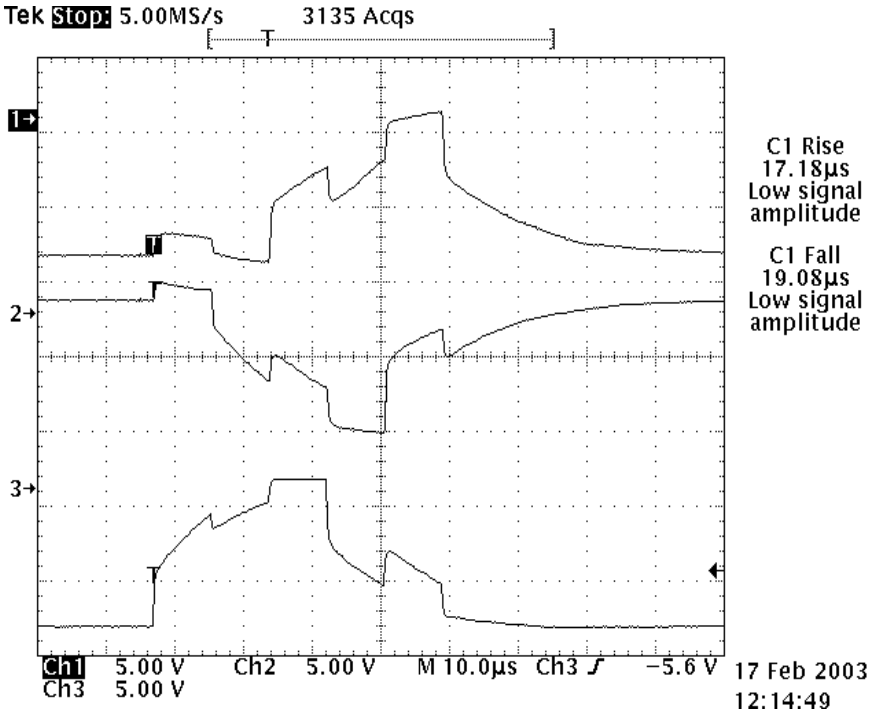


Figure 6.9: Four loads (two non-frame-transfer CCDs)

Note : The rise time is greater than the pulse width, the clock pulse never reaches the high voltage , thus the indicated rise time is unreliable.

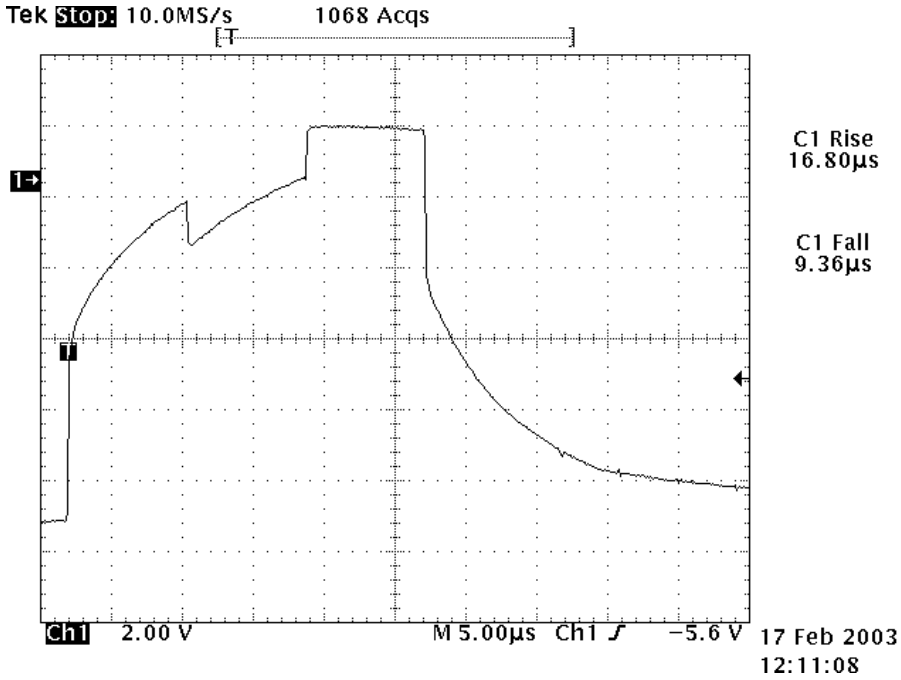


Figure 6.10: Detail of waveform in Figure 6.8. Two loads

T_r: 17µs; T_o: 8µs: this does not comply with the E2V specification of $T_r < 0.5\ T_o$.

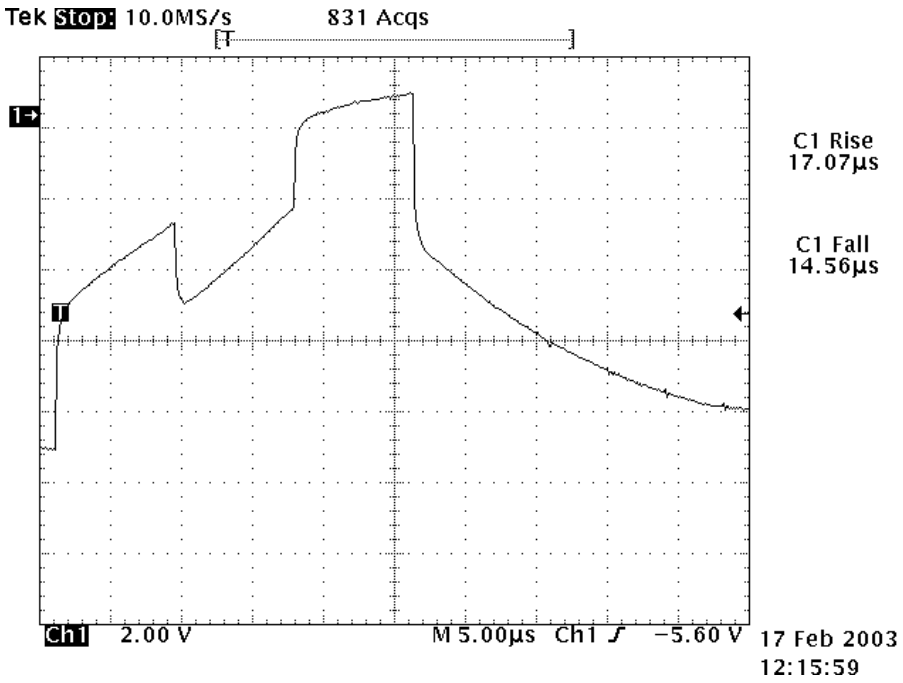


Figure 6.11: Detail of waveform in Figure 6.9. Four loads

T_r: unreliable; T_o: 8µs: this does not comply with the E2V specification of $T_r < 0.5\ T_o$.

6.4.3 Tabulated Results

Table 1: Clock Pulse width T_w = 50µs; Triplet time T_i = 100µs

Loads	Rise Time T_r(µs)	Fall Time(µs)	Overlap T_o(µs)	Comments
1	4.98	4.74	16.6	T_r <0.5 T_o. In spec.
2	13.3	10	16.6	T_r >0.5 T_o. Out of spec.
3	28	14.7	16.6	T_r >0.5 T_o. Out of spec.
4	33.4	19.5	16.6	T_r >>0.5 T_o. Out of spec.

Table 2: Clock Pulse width T_w = 25µs; Triplet time T_i = 50µs

Loads	Rise Time T_r(µs)	Fall Time(µs)	Overlap T_o(µs)	Comments
2	16.8	9.4	8.3	T_r >0.5 T_o. Out of spec.
4	Unreliable	14.6	8.3	T_r >>0.5 T_o. Out of spec.

6.5 Discussion

Private communication with Dr Paul Jorden of E2V indicates that reducing clock pulse width and hence row transfer time is acceptable for small signals so long as the amplitude does not reduce (i.e. rise/fall time greater than width).

Figures 9 & 11 show a condition where the rise time for four loads exceeds the pulse width of 25µs making the oscilloscope calculated rise/fall time numbers unreliable.

The PFIS detector preliminary design documentation used a row transfer time of 50µs for readout time calculations, giving total row transfer time for full frame readout of:

4102 x 50µs = 205ms

The E2V data sheet for the CCD4482 recommends the following:

Table 3: E2V datasheet values (all times in µs)

	Minimum	Typical	Maximum
Row transfer T_I	50	100	
Pulse width T_w	25	50	
Rise time T_r	1	10	0.5 T_o
Overlap T_o	5	10	0.2 T_i

According to the datasheet, only one of the tabulated test results is acceptable – that of one load with 50µs pulse width, as shown in Figure 6.4. However, many groups use the SDSU controller to drive E2V 2Kx4K detectors, most configure their systems as one detector per clock driver output, equating to the two-load test described above. Thus we can safely assume that the two-load option gives acceptable performance in spite of not conforming to the E2V datasheet requirements.

In the case of the PFIS detector system, to comply with the $T_r < 0.5\ T_o$ specification using one clock board, the clock pulse width will have to be extended as follows:

Three load T_r: 28µs

Overlap required: $2 \times T_r = 56$µs

Thus row transfer time T_i: 56/0.2 = 280µs

Total row transfer time for image readout: 280µs x 4102 = 1.15 seconds

This is unacceptably long.

However, from discussions with Dr Paul Jorden it seems that the E2V specifications are very conservative, and applicable to large signal levels.

6.6 Conclusion/Recommendation

To guarantee best performance (fastest row transfer times in readout) the PFIS detector system must use the large SDSU controller crate with three clock boards.

Use of the small SDSU controller crate will result in slower row transfer times due to the SDSU clock driver board limitations when driving high capacitance loads. I estimate that the reduced performance will be approximately

100µs/row = 410ms image transfer time

for high signal levels. It should be possible to achieve satisfactory performance with faster row transfer times for small signal levels – this is difficult to quantify without more exhaustive tests.

A decision must be made on the trade-off between the best performance achievable with the larger/heavier controller and slower row transfer times obtained with the standard size controller crate. The following information is pertinent to this decision:

Mass/size comparison

	Small crate	Large crate	Small PSU	Large PSU
Mass (Kg)	6.4	9.7	5.4	7.95
Length (mm)	333		230	
Width (mm)	162		200	
Height (mm)	140		110	

Note: these dimensions do NOT include the volume required for cabling/connectors.

Cost comparison

Small crate system	Large crate system
$29200	$35200.00

Note: These prices are to be confirmed

Small crate system details:

1 x ARC-70 6-slot housing	$2000
1 x ARC ?? Large power supply	$2000
1 x ARC-22 250MHz timing board	$2500
1 x ARC-50 utility board	$2000
3 x ARC-45 differential video board	$15000
1 x ARC-30 clock board	$2500
1 x ARC-64 250MHz PCI board	$3000
1 x 100m optical fibre	no charge
1 x watercooled heat exchanger	$200
TOTAL	**$29200**

Large crate system details:

1 x ARC-?? 12-slot housing	$3000
1 x ARC ?? Large power supply	$2000
1 x ARC-22 250MHz timing board	$2500
1 x ARC-50 utility board	$2000
3 x ARC-45 differential video board	$15000
3 x ARC-30 clock board	$7500
1 x ARC-64 250MHz PCI board	$3000
1 x 100m optical fibre	no charge
1 x watercooled heat exchanger	$200
TOTAL	**$35200**

7 Sub-Systems Controller

The sub-systems controller consists mainly of a multi-function analog/digital controller originally developed by the SAAO for the InSb infrared camera. Communication from the PFIS computer to the sub-systems controller is via the SDSU controller and its RS-232 port on the utility board. All connections between the SDSU controller and the sub-systems controller are optically isolated. The sub-systems controller and the sub-systems it controls are powered from the sub-systems power supply. The sub-systems controller controls the following PFIS sub-systems:

7.1 Temperature Monitoring

The sub-systems controller can monitor two temperature points inside the cryostat. The one temperature point will be on the cold plate and the other TBD2. The sub-systems controller will also control the cold plate heater.

7.2 Varian Ion Pump

A Varian Ion Pump unit is used to maintain the cryostat vacuum integrity. The ion pump will also function as a vacuum gauge to allow long-term monitoring of the state of the cryostat vacuum to facilitate maintenance planning. On/Off control of the ion pump and the acquisition of the vacuum reading from the ion pump will be via the sub-systems

controller. The sub-systems controller will also be able to verify the on/off state of the ion pump.

7.3 EMI Protection of Signals

The control signals to and from the sub-systems controller and the sub-systems it controls might be susceptible to electromagnetic interference (EMI). The level of interference will be very low as the length of the cables carrying these signals will be short (less than 2 meters) and the control signals will be of a low frequency. To reduce the level of interference all cables carrying control signals between the sub-system controller and the sub-systems it controls will be screened. As an added measure of protection the option of either low-pass filters and/or transient suppressors on the control lines or a de-bounce algorithm in the sub-system controller software controlling the sub-systems will be taken under advisement.

8 Mosaicing

The PFIS detector subsystem is based on three E2V CCD44-82 CCD chips mounted on a common cold plate. Mosaicing consists of:

- Measuring and correcting the co-planarity of the three CCD detector chips.
- Measuring and correcting the row offset between adjacent CCD chips.
- Measuring and correcting the degree of rotation between adjacent CCD chips.

This document describes the plan for mosaicing the PFIS detector chips and draws heavily on the document “CCD Mosaicing” by W.P.Koorts, SAAO.

8.1 Functional Requirements

CCD mosaicing involves the mounting two or more CCDs such that their detection surfaces are co-planar between individual CCDs as well as to a reference (mounting) plane. It is also necessary to align the rows between individual CCDs and also adjust the amount of rotation between CCDs to get the columns parallel to each other.

CCDs are typically mounted on an Invar “cold plate” which acts as both a thermal sink for cooling as well as a stable platform for holding the mosaic. Each CCD is mounted on three pedestals that are shimmed to the exact height to get the CCDs co-planar at some fixed distance above the cold plate.

The reference plane can be either the mounting surface of the cold plate or a reference surface on an attached mounting jig used to accurately position the mosaic in the cryostat.

8.2 Mosaicing a Detector System

The first requirement is a clean room temperature controlled to 20C to ensure the cleanliness of the CCDs. An Electrostatic Discharge (ESD) station is necessary to protect the CCDs from potentially destructive static electricity.

The measuring equipment consists of:

- A stable surface (granite slab) and frame to support cold plate and measuring equipment.
- An automated X-Y Positioning Table calibrated in the Z direction.
- A Laser Displacement Sensor capable of measurements < 1 micron for mosaic flatness measurements.
- A suitable imaging system for row offset and rotation measurements and adjustments.

The mosaicing process consists of accurately measuring a matrix of points on the 3 CCDs mounted on the cold plate. The measurements obtained are analysed to obtain the mean plane of each CCD. The CCDs are then adjusted by precision grinding or lapping of the shims to the exact size required to get the CCDs coplanar.

8.3 Mosaicing Specifications

8.3.1 CCD44-82 Physical Dimensions

The E2V CCD44-82 has 4k +6 rows of light sensitive pixels.

ie. 4096+6 = 4102 pixels

Detector "height" (sensitive pixels) is therefore 4102*15micron = 61.53mm

Top inactive edge spacing is nominally 0.16micron

Bottom inactive edge spacing is nominally 5.0mm

Total CCD physical height = 61.53mm+0.00016mm+5.0mm = 66.53mm

The "width" image area per CCD is 2048*15micron = 30.72mm

Left and right inactive edge spacing per CCD is nominally 0.5mm

The gap between packages is nominally 0.5mm

Total physical "width" = 93.16mm

8.3.2 E2V CCD44-82 Flatness specification

The silicon flatness specification obtained from E2V is ±10 micron.

ie. 20 micron peak-to-valley.

E2V are confident that they can deliver CCDs that are flat to ±7.5 micron

ie. 15 micron peak-to-valley.

8.3.3 E2V CCD44-82 Reflectivity

With astro-broadband coating surface reflectivity at 670nm (red) is about 10%.

8.3.4 Specifications for the assembled PFIS mosaic:

Required Flatness:	± 10 micron for the entire mosaic.
Maximum Row offset:	6 pixels (15 microns/pixel *6 = 90 microns)
Column Alignment:	±5 pixels in 4096

8.4 Mosaicing Procedure

A granite slab supports the XY table. A displacement sensor mounted on the XY table measures vertically upward to either a reference surface or the mosaiced CCDs supported by the stable frame.

The XY table is characterized in Z for all XY positions of interest using a reference surface mounted in the frame at the nominal sensing distance of 30mm.

The mosaiced CCDs in their mounting jig are then positioned in the stable frame and the Z distance to each of the CCDs is measured at a number of XY positions. Distance measurements are also taken to the three reference mounting pads on the cold plate mounting jig.

On a 2k x 4k CCD E2V measures 9 points, one in the center, one in each corner and one between each of the four corner points whereas ESO typically measures 100 evenly distributed points.

The mean plane of the cold plate, represented by the three reference pads as well as the mean plane of each CCD, can now be obtained by software analysis of the data.

From this information the precise shim lengths can be calculated.

By precision grinding and measuring with a laser micrometer the 9 CCD shims can be adjusted to get the three CCDs coplanar with each other and with the reference plane.

The measurement and shimming process may have to be done iteratively to prevent overshooting the required position.

9 List of TBC Issues

TBC1 - Readout noise of 3 and 5 e^-/pix at readout rates of 100 and 333 kHz

TBC2 - Pixel readout overhead for 2x2 compared with 1x1 prebinned readout

TBC3 - Readout rates in the range 100-333 kHz

TBC4 - Pixel skip times are 1.0 μsec/pix

TBC5 - Additional overhead for each increment in prebinning is 1.0 μsec

TBC6 - Number of windows allowed

TBC7 - Very high speed spectroscopic performance

TBD1 - Base gain of electrons/ADU

TBD2 - Second temperature point inside cryostat