Southern African Large Telescope
SALTICAM
Preliminary Design Review

Document Number 3360AE0001:
Detector Document

Darragh O'Donoghue
Dave Carter
Geoff Evans
Willie Koorts
James O'Connor
Faranah Osman
Stan van der Merwe

Revision 1.5
31 January 2002

Table of Contents

1 Scope 2
2 Overview 3
3 The CCDs 3
3.1 Basic Parameters 3
3.2 Sensitivity 4
3.3 Frame Transfer Architecture 5
3.4 Mini-Mosaic 5
3.5 Cosmetics 6
3.6 Dark Current and Operating Temperature 6
3.7 Readout Noise 6
4 CCD Controller 7
4.1 Readout Speed 7
4.2 Lowest Noise Full Frame Readout 7
4.3 Rapid Full Frame Readout 8
4.4 Prebinning 8
4.5 Frame Transfer Operation 8
4.6 Windowing: Slot Mode And Autoguiding 9
4.7 Gain 10
5 List of TBC Issues 10

1 Scope

This document reports a design study carried out for the preliminary design review of SALTICAM, the verification instrument, acquisition camera, and scientific imager of the Southern African Large Telescope (SALT). It will describe how the design of the detectors described in the other documents was reached.

CCD procurement was recognized to be a long lead time purchase and a contract was concluded with Marconi Applied Technologies in January 2002 to secure devices for the two SALT first light instruments.

2 Overview

The detector subsystem will comprise a cryostat containing a 2x1 mini-mosaic of CCD chips. These chips shall be Marconi Applied Technologies 44-82 CCDs with 2k x 4k x 15 micron pixels. They shall be mounted on an invar cold plate and in the baseline design, it is planned that Marconi will do the butting in order to achieve co-planarity of the devices. (It is possible that SAAO may undertake the butting if feasible technically, financially and in terms of the schedule). The mosaic shall be housed in an evacuated cryostat and thermally connected to the cold end of a Cryotiger, which shall cool the chips sufficiently to render dark current insignificant, whilst at the same time reducing QE by the smallest extent possible. The detectors shall be managed by an SDSU II CCD controller, which will in turn be controlled by a PC.

3 The CCDs

In terms of a contract between the SALT Foundation and Marconi Applied Technologies (hereafter Marconi), the latter will supply their CCD 44-82 chips for use as the SALTICAM detectors. Marconi currently offer the best performance in astronomy grade devices of any *commercial* manufacturer. Possibly better performance at cheaper cost is available from Lincoln Lab/MIT chips, but these devices are supplied to consortia and are not routinely available commercially. As a result, delivery is too risky. The decision not to pursue the Lincoln Lab/MIT chips was endorsed by the SALT Science Working Group at the PFIS PDR in October 2001 in Madison, Wisconsin, USA.

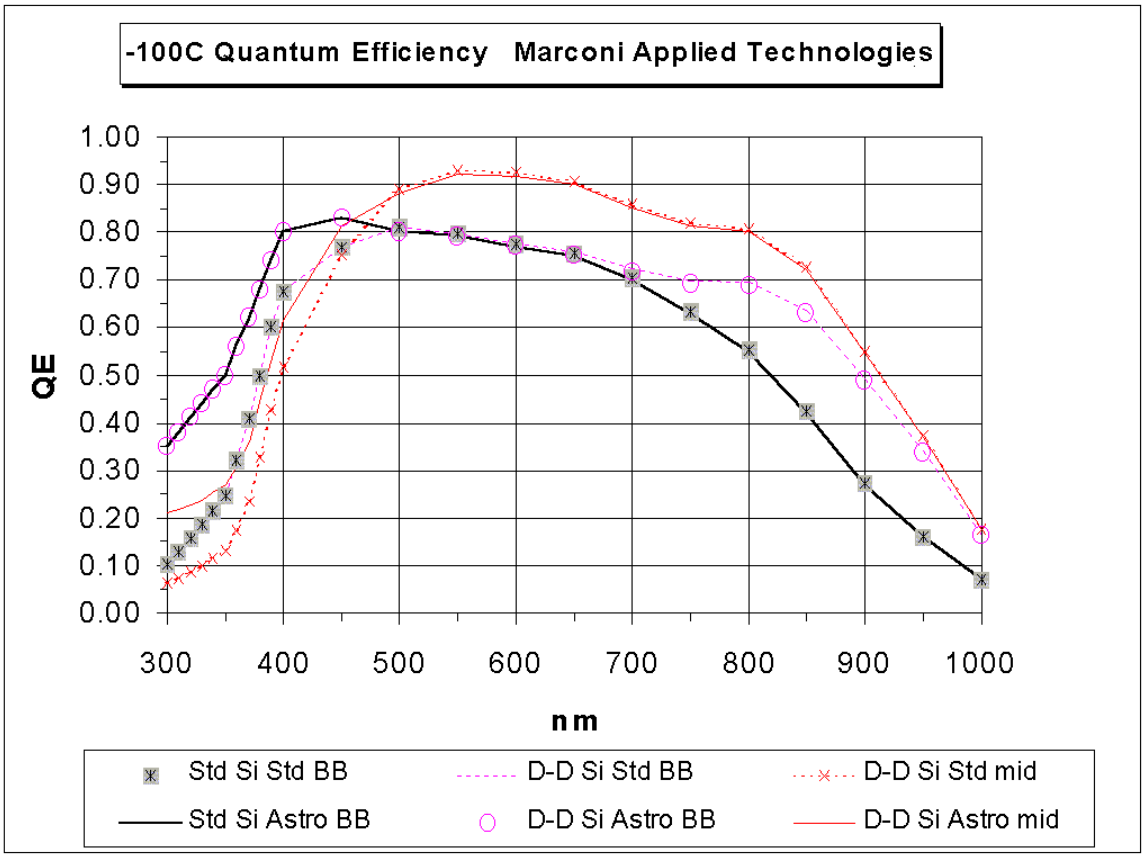
During CCD procurement, the capabilities of SITe chips were revisited. A new 2k x 4k x 15 micron SITe CCD is currently in the final stages of development, with final performance specifications to be issued in February 2002. However, it is not available with Frame Transfer capability. Because of this, uncertainties in performance which would only be defined when it was too late to purchase Marconi CCDs, and the generally mediocre reputation that SITe enjoys at SAAO for delivery to specification, the SALT CCD Procurement Forum agreed not to pursue SITe chips.

3.1 Basic Parameters

The CCD characteristics may be obtained from the Marconi data sheets, the most important details of which are reproduced below. In this list, guaranteed (min or max as appropriate) as well as (more generous) typical figures are quoted:

- 2048 x 4096 x 15 micron square pixels
- 30.7 x 61.4 mm^2 imaging area
- Thinned and back-illuminated
- 3-side buttable

- 2 output amplifiers
- Charge transfer efficiency: min: 99.999 per cent, typical 99.9995 per cent
- Pixel readout frequency 20-1000 kHz
- Peak signal (full well): min: 150 k e^-/pix, typical: 200 k e^-/pix
- Readout noise (at 188 K, 20 kHz): max: 4.0 e^-/pix, typical: 2.5 e^-/pix
- QE at 500 nm: typically 80 per cent
- Spectral range: 200-1060 nm
- Dark current (at 153 K): max: 4, typical: 0.1 e^-/pix/hr



3.2 Sensitivity

Dr. Paul Jorden of Marconi Applied Technologies has provided the above plot showing typical performance for Marconi devices (this plot was used for discussion with the UK Vista Survey telescope project about their CCD requirements). In the legend, BB denotes

Broad Band coating and D-D denotes deep depletion silicon, which extends red response without compromising the blue. The D-D silicon and the Astro BB type of anti-reflection coating option has been selected for SALTICAM.

However, it must be remembered that the plot shows “typical” performance figures (i.e. the mean of a large sample of Marconi devices). Any specific device may not achieve this performance. Marconi have undertaken to guarantee minimum performance as specified in the table below, shown alongside the “typical” sensitivity for comparison (these figures apply to deep depletion silicon devices, combined with the Astronomy Broad-Band Anti-reflection coating):

Table 1 CCD Sensitivity

Wavelength	Spectral Response (QE)	
(nm)	Min	Typical
350	40	50
400	70	80
500	75	80
650	70	75
900	45	50

3.3 Frame Transfer Architecture

In order to enable rapid imaging, FT operation is essential. None of the large format devices made by Marconi Applied Technologies are available off the shelf in Frame Transfer (FT) Mode. Marconi are to supply FT chips in terms of the contract with SALT. This requires a redesign of the clock lines of the chip and therefore a special production run from Marconi. The delivery time to complete the order for SALTICAM devices is 10 months.

3.4 Mini-Mosaic

A mini-mosaic of 2x1 CCDs will be used. Butting will probably be carried out by Marconi who offer co-planarity of the devices to better than 10 microns. Costs of this are still awaited.

3.5 Cosmetics

In terms of the contract between SALT and Marconi, the latter may supply grade 0 (preferably) or grade 1 (minimum) devices. The numerical definition of these specifications is shown in the following table:

Table 2 CCD Grade Blemish Specification

Defects	Grade 0	Grade 1
Column defects (black or white)	6 or less	12 or less
White spots	500 or less	1000 or less
Total spots (black or white)	1250 or less	2000 or less
Traps	30 or less	50 or less

3.6 Dark Current and Operating Temperature

The performance goal for dark current is to ensure that noise on the dark current pedestal generated during the longest exposure is small compared to the readout noise. We estimate that, with minimum readout noise of 2.5 e^-/pix, a dark current rate of 1 e^-/pix/longest exposure will fulfill this satisfactorily. The longest exposure is expected to be about 1 hr. So a dark current rate of less than 1 e^-/pix/hr at 160 K is required, and promised in terms of the Marconi contract with SALT.

3.7 Readout Noise

In terms of their contract with SALT, Marconi guarantee a readout noise from the on-chip amplifier of 4.0 e^-/pix at a readout speed of 20 kHz. 2.5 e^-/pix is typical. A plot in the Marconi data sheet shows how the readout noise increases with readout speed. We expect the SDSU II controller and additional electronics to add 1.5 e^-/pix (assuming a gain of 1 e^-/ADU). We thus propose the following readout noise performance:

- 3.3 e^-/pix at 100 kHz (10.0 μsec/pix)
- 5.0 e^-/pix at 333 kHz (3.0 μsec/pix)

These values depend on the devices supplied by Marconi and are in any case **TBC1**.

4 CCD Controller

The CCD controller will be an SDSU II (Leach) controller from Astronomical Research Cameras (San Diego). The controller will have 4 video channels allowing the use of two outputs per CCD chip.

4.1 Readout Speed

Marconi certify performance in the range 20-1000 kHz. The SDSU II controller allows readout rates of no more than 1000 kHz.

Due to difficulties with getting the SDSU controller working with a PCI card running in a PC, as well as needing real Marconi chips with which to conduct tests, we will use performance estimates from Guy Woodhouse, a CCD engineer we know well who worked on La Palma and now works on the fast CCD camera for the Faint Object Spectrograph for Subaru. Guy has solid experience with the same kind of Marconi chips and SDSU controllers. For the present, we thus aim to match the performance he reports.

Correlated Double Sampling (CDS) speeds of 3.0 μsec/pix (at 5 e^-/pix readout noise) have been achieved with the proposed chips and SDSU controllers by Guy. It may be possible to reduce the 3.0 μsec/pix (with readout noise penalty) but this remains to be investigated. Prebinning and/or windowing causes the figures to increase somewhat (**TBC2**) (from 3.0 to 4.0 μsec/pix).

We therefore propose a discrete set of normal pixel readout rates in the range 100-333 kHz (**TBC3**) and software selectable (slower readout rates would result in unacceptably long readout times). In addition, drift scan and charge shuffling during exposure will require special control of the vertical clocks which will be synchronized at a software selectable rate.

Overheads are also associated with row transfers, 50 μsec per row, and pixel skips (discards) of 0.8 μsec/pix (**TBC4**).

Each CCD has 4096 rows, 2048 columns and 2 readout amplifiers. There are an additional 50 pixels at the end of each readout register but before the readout amplifier. Thus, readout requires feeding 4096 rows of (1024+50) columns, or a total of 4399104 pixels, through each readout amplifier.

4.2 Lowest Noise Full Frame Readout

Lowest readout noise is expected at the slowest readout rate of 100 kHz (10 μsec/pix). Readout times at this rate would be:

- **Time to clear the chip prior to exposure or time for vertical transfers during readout: 4096*50 μsec = 0.205 sec**

- **Time to read out the full chip (without prebinning):**
  0.205 sec + 4399104*10.0 μsec = 44.196 sec (readout noise of 3.3 e^-/pix: TBC1)

4.3 Rapid Full Frame Readout

The above timing considerations give rise to the following expected performance when high time resolution is desired:

- **Minimum time to read out the full chip (without prebinning):**
  0.205 sec + 4399104*3.0 μsec = 13.402 sec (readout noise of 5 e^-/pix)

Readout time can be decreased further by any one of (or combinations thereof):

- Frame transfer operation so that only half the detector is used. There is no readout dead time as the next exposure is accumulating during the readout.
- Prebinning (see next section)
- Windowing of the chip either in the spatial or wavelength direction or both

4.4 Prebinning

Software-selectable prebinning of 1x1 to 9x9 (independent in each dimension) will be offered. For all but the highest resolution observations, 2x2 prebinning will be used. Such prebinning will then result in minimum readout times of:

- **2x2 prebinning: 0.205 sec + 1099776*10.0 μsec = 11.203 sec (3.3 e^-/pix readout noise: TBC1)**
- **2x2 prebinning: 0.205 sec + 1099776*4.0 μsec = 4.604 sec (5 e^-/pix readout noise)**

We believe that there will be increased overhead with increasing prebinning so readout rates for higher than 2x2 prebinning are currently unknown. We believe there will be a 1 μsec overhead for each prebinning increment (essentially the time to combine pixels during readout). However, this is **TBC5**.

4.5 Frame Transfer Operation

Frame Transfer capability will be provided by the CCD controller. In this mode, at the end of an exposure of the half of the chip furthest from the readout register (the image section of the chip), the data are rapidly shifted (in 0.102 sec) into the half of the chip next to the readout register (the store section). Readout of the store section then takes place. Naturally, the store section of the chip must be masked from light so that half the science FoV must be sacrificed. The shutter is open throughout the sequence of operations.

Minimum readout times are (with 4096 vertical transfers required because although only 2048 are required to move the image into the store area, vertical transfers in the store area are still required):

- **2x2 prebinning: 4096*50 μsec + (537*1024*10.0) μsec = 5.704 sec (3.3$^-$/pix readout noise).**
- **2x2 prebinning: 4096*50 μsec + (537*1024*4.0) μsec = 2.404 sec (5 e$^-$/pix readout noise).**

Thus, a continuous sequence of images with, say, 2.6 sec sampling (allowing 0.2 sec for overhead) and no dead time can thus be obtained. Image smearing will occur during the 0.102 sec needed for frame transfer.

4.6 Windowing: Slot Mode And Autoguiding

Readout of up to 10 windows (**TBC6**) of rectangular shape and arbitrary size will be offered by the CCD controller. Note that a window defined on one half of one CCD chip is also applied to the other half, as well as replicated twice on the other chip. This is because the readout through each amplifier must use the same clocking scheme.

Two examples will illustrate the readout rate possible with windowed operation. The performance in these examples must certainly be confirmed (**TBC7**).

In the first, an image is to be obtained of a point source located near the middle of the chip, just above the frame transfer boundary. The full width of the detector parallel to the frame transfer boundary is to be used. Perpendicular to the frame transfer boundary, 960 microns (64 pixels) corresponding to 8.97 arcsec on the sky is to be used. Assuming frame transfer operation and 2x2 prebinning, the minimum readout time would be:

$$0.105 \text{ sec} + (32*537*4.0)\ \mu\text{sec} = 0.174 \text{ sec}$$

where the first contribution (0.105 sec) is the time taken to shift the image down by roughly half a frame (to the readout register). The second contribution (0.069 sec) is the time taken to read out the 32 x 537 pixels. However, the image would be exposed for only 0.069 sec and there would be 0.105 sec during which the image would be smeared. This is unacceptable.

The 0.105 sec contribution could be reduced, thereby yielding imaging at a speed of about 10 Hz, if the image is shifted just over the frame transfer boundary, rather than all the way down to the readout register. The minimum readout time would then be:

(64*50) μsec + (64*50) μsec + (32*537*4.0) μsec

= 0.0032 sec + 0.0032 sec + 0.069 sec

= 0.076 sec

A sequence of such images could then be obtained with a cycle time of **0.1 sec** (allowing 0.025 seconds for safety for image storage – this could possibly be reduced) and image

smearing over a 0.0032 sec interval. Thus, image strips of 64 rows would migrate to the readout register where they would appear some time after exposure. Management of time stamping will need to be carefully handled. Further discussion of slot mode appears in 3300AE0005 OCDD.pdf.

The second example is an imaging example in which a target and two comparison stars are to be sampled rapidly by reading out three 128x128 boxes of pixels centred on the three objects. In full frame mode (i.e. shuttered), but 2x2 prebinning, the minimum readout time would involve 0.205 sec for vertical transfers, (3*64*(537-64)*0.8) μsec for pixel skipping and (3*64*64*4.0) μsec for pixel reads. These contributions are:

0.205 sec + 0.073 sec + 0.049 sec = 0.322 sec

once again dominated by the time for vertical transfers. Frame transfer operation would cut this time in half.

4.7 Gain

The SDSU controller allows the gain to be scaled by one of four preset factors: x1; x2; x4.75; x9.5. The base gain can be set by adjusting the electronics and this is still to be decided: **TBD1**.

5 List of TBC Issues

TBC1 - Readout noise of 3.3 and 5 e^-/pix at readout rates of 100 and 330 kHz

TBC2 - Pixel readout overhead for 2x2 compared with 1x1 prebinned readout

TBC3 - Readout rates in the range 100-330 kHz

TBC4 - Pixel skip times are 0.8 μsec/pix

TBC5 - Additional overhead for each increment in prebinning is 1.0 μsec

TBC6 - Number of windows allowed

TBC7 - Very high speed imaging performance

TBD1 - Base gain of electrons/ADU