

80 MHz Monolithic CMOS Triple 8-bit VIDEODAC™

Distinguishing Features

- 80, 50 MHz Operation
- Triple 8-bit D/A Converters
- Optional Internal Voltage Reference
- RS-343A-Compatible Outputs
- TTL-Compatible Inputs
- +5 V CMOS Monolithic Construction
- 44-pin PLCC Package
- Typical Power Dissipation: 600 mW

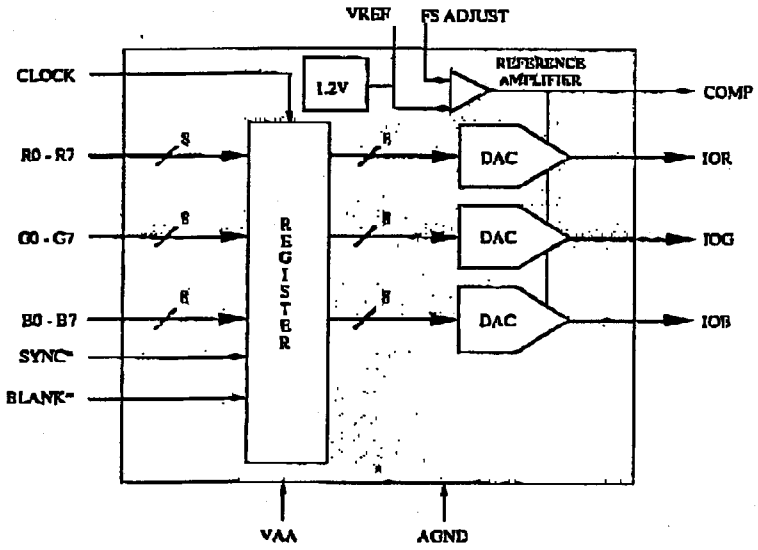
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Instrumentation

Related Products

- Bt473

Functional Block Diagram



Product Description

The Bt121 is a triple 8-bit VIDEODAC designed specifically for high-performance, high-resolution color graphics.

This device offers a higher level of integration than previous VIDEODAC designs. Included is an on-chip voltage reference to simplify use of the device.

The Bt121 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load, and RS-170-compatible video signals into a singly-terminated 75 Ω load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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Circuit Description

As illustrated in the functional block diagram, the Bt121 contains three 8-bit D/A converters, input registers, and a reference amplifier.

On the rising edge of CLOCK, 24 bits of color information (R0–R7, G0–G7, and B0–B7) are latched into the device and presented to the three 8-bit D/A converters.

Latched on the rising edge of CLOCK to maintain synchronization with the color data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as illustrated in Figure 1. Table 1 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt121 use a segmented architecture in which bit currents are routed to either the output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt121 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

ESD and Latchup Considerations

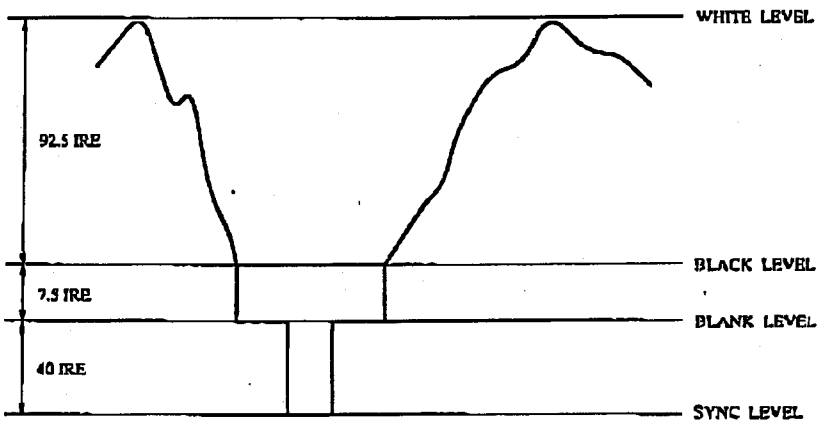
Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET ~ 143 Ω, and VREF = 1.23 V. RS-343A levels and tolerances are assumed on all levels.

Figure 1. Composite Video Output Waveforms.

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK - SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: 75 Ω doubly-terminated load, SETUP = 7.5 IRE. VREF = 1.23 V and RSET ~ 143 Ω.

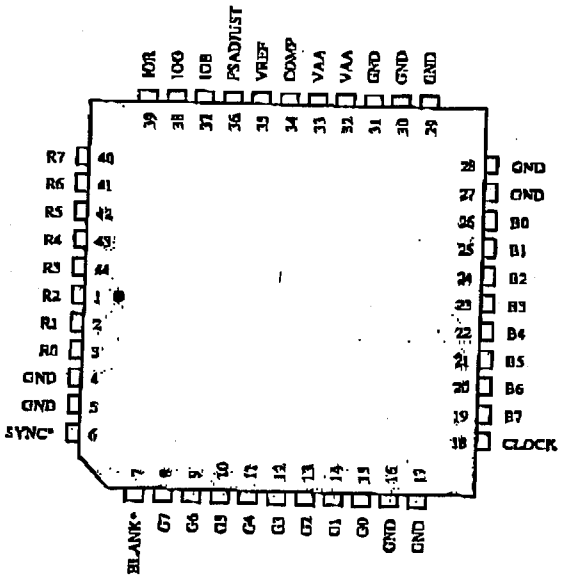
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOR, IOG, and IOB outputs to the blanking level, as detailed in Table 1. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the R0–R7, G0–G7, and B0–B7 inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOR, IOG, IOB outputs (see Figure 1). SYNC* does not override any other control or data input, as shown in Table 1; therefore, SYNC* should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
R0–R7, G0–G7, B0–B7	Red, green, and blue data inputs (TTL compatible). R0, G0, and B0 are the least-significant data bits. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (see Figures 2 and 3 in the PC Board Lay-out Considerations section). All outputs, whether used or not, should have the same output load.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 1). The IRE relationships in Figure 1 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOR, IOG and IOB is: RSET (Ω) = K * VREF (V) / IO (mA) Where; K = 2,295 with SYNC*=0 K = 3,195 with SYNC*=1

Pin Descriptions *(continued)*

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor in series with a resistor should be connected between this pin and the nearest VAA pin (Figures 2 and 3) for optimum settling time. Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.
VREF	Voltage reference input. If an external voltage reference is used (Figure 3), it must supply this input with a 1.2 V (typical) reference. A 0.1 µF ceramic capacitor must always be used to decouple this input to GND, as shown in Figures 2 and 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When the internal reference is used, this pin should not drive any external circuitry, except the decoupling capacitor (Figure 2).
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	V
50, 35 MHz Parts		4.5	5.00	5.5	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
External Reference Voltage	VREF	1.11	1.235	1.36	V
FS ADJUST Resistor	RSET		143		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND– 0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the absolute maximum ratings (especially relative to VAA or between VAA pins) can induce destructive latchup.

DC Characteristics

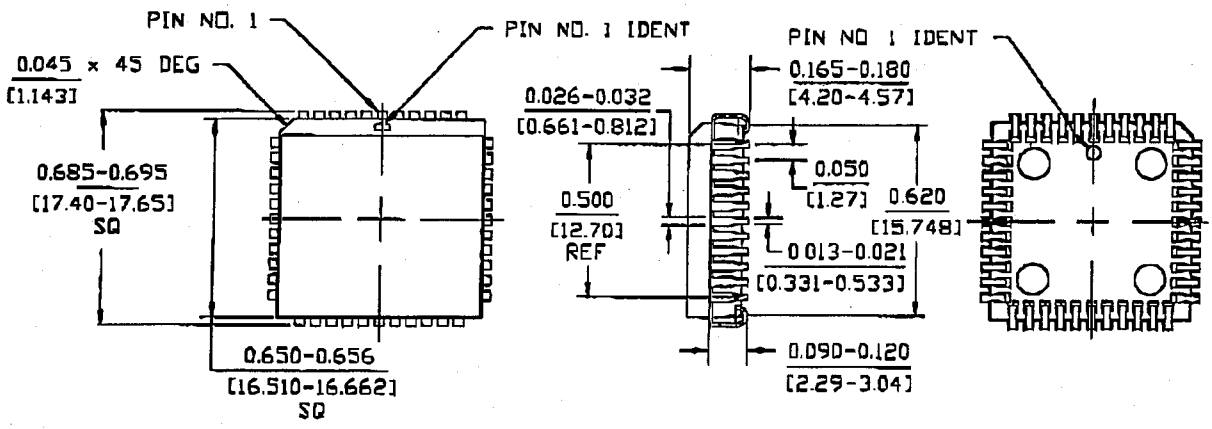
Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error					
External Reference				±5	% Gray Scale
Internal Reference				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Output					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 400 µA)	VOL			0.4	V
Output Capacitance	CDOUT			7	pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Sync Level on IOR, IOG, IOB		6.29	7.62	7.94	mA
LSB Size			69.72		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.4	V
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		30		pF
Internal VREF Voltage Range	INTVREF	1.08	1.2	1.32	V
Internal VREF Output Current	IVREF			10	µA
Power Supply Rejection Ratio (Note 1) (COMP = 0.01 µF, f = 1 kHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 143 Ω, and VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

When the internal voltage reference is being used, RSET may require adjustment to meet these limits.

Note 1: Guaranteed by characterization, not tested.

Package Drawing—44-pin Plastic J-Lead (PLCC)



Notes: Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ±0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.